TAU 2013 – Program

http://www.tauworkshop.com
March 27–29, 2013
Ridge Tahoe Resort (Lake Tahoe)
Stateline, Nevada, USA

Wednesday, March 27, 2013

11:00 a.m. – 12:00 p.m. TAU/ISPD Joint Session on Contests *(Chair: Charles Liu, TSMC)*

The ISPD 2013 Discrete Gate Sizing Contest and Benchmark Suite
Muhammet Mustafa Ozdal, Chirayu Amin, Andrey Ayupov, Steven Burns, Gustavo Wilke, Cheng Zhuo (Intel)

The TAU 2013 Variability Aware Timing Analysis Contest
Debjit Sinha[1], Luis Guerra e Silva[2], Jia Wang[3], Shesha Ragunathan[1], Dileep Netrabile[1], Ahmed Shebaita[4]
[1]IBM, [2]INESC-ID / IST - TU Lisbon (Portugal), [3]Illinois Institute of Technology, [4]Synopsys

12:10 p.m. – 1:30 p.m. TAU/ISPD Keynote and Lunch *(Chair: Chirayu Amin, Intel)*

Opportunities and Challenges for High Performance Microprocessor Designs and Design Automation
Dr. Ruchir Puri (Fellow, IBM)

1:30 p.m. – 1:45 p.m. Break

1:45 p.m. – 2:00 p.m. TAU 2013 Opening remarks by Jinjun Xiong (IBM), TAU General Chair

2:00 p.m. – 3:30 p.m. TAU/ISPD Invited Session: What will it take to tame the hierarchical design trolls? *(Chair: Tom Spyrou, Altera)*

To do or not to do Hierarchical Timing?
Florentin Dartu and Qiuyang Wu (Synopsys)

Variability Aware Hierarchical Implementation of Big Chips
Vidyamani Parkhe (Mentor Graphics)

Challenges in Managing Timing and Wiring Contracts during Hierarchical Floorplanning and Design Closure
Shyam Ramji (IBM)

3:30 p.m. – 4:00 p.m. Break

4:00 p.m. – 5:30 p.m. EDA Court: Hierarchical Construction and Timing Sign-Off of SoCs
Judge: Chandu Visweswariah (IBM)
Plaintiffs: Amit Shaligram (ST Microelectronics), Guntram Wolski (Cisco), Larry Brown (IBM), Oleg Levitsky (Cadence)
Defendants: Alex Rubin (IBM), Alexander Skourikhin (Intel), Igor Keller (Cadence), Qiuyang Wu (Synopsys)

6:30 p.m. – 7:30 p.m. Hors D'oeuvres (Appetizers)

Sponsors:

Thursday, March 28, 2013

8:30 a.m. – 9:00 a.m. Breakfast

9:00 a.m. – 10:30 a.m. Analog and Mixed Signal CAD *(Chair: Duaine Pryor, Mentor Graphics)*

Bayesian Model Fusion: Large-Scale Performance Modeling of Analog and Mixed-Signal Circuits by Reusing Early-Stage Data
Fa Wang[1], Wangyang Zhang[1], Shupeng Sun[1], Xin Li[1], Chenjie Gu[2]
[1]Carnegie Mellon University, [2]Intel

A Formal Approach to DC Operating Point Analysis for Large Mixed Signal Circuits: Challenges and Opportunities
Parijat Mukherjee[1], Chirayu Amin[2], Peng Li[1]
[1]Texas A&M University, [2]Intel

ABCD-D: Accurately Capturing Analog Effects in Digital Components using Finite State Machine Models
Karthik Aadithya, Jaijeet Roychowdhury (University of California, Berkeley)

10:30 a.m. – 11:00 a.m. Break

11:00 a.m. – 12:00 p.m. Panel: Variability in Timing: Where is Statistical Timing?
Organizer and Moderator: Igor Keller (Cadence)
Panelists: Anthony Hill (Texas Instruments), Debjit Sinha (IBM), Florentin Dartu (Synopsys), Hidetoshi Onodera (Kyoto University)

12:00 p.m. – 1:30 p.m. Lunch

1:30 p.m. – 2:30 p.m. Keynote *(Chair: Chirayu Amin, Intel)*

Unsolved Problems in Static Timing Analysis: A Challenge
Tom Spyrou (Design Technology Architect, Altera)

2:30 p.m. – 3:30 p.m. TAU-20 Talks *(Chair: Hidetoshi Onodera, Kyoto University)*

Signal Integrity Analysis in 20nm and Below: Challenges and Advances
Igor Keller (Cadence)

Multi-synchronous Approaches to Derive Energy and Architectural Benefits in Clocked Peripherals
William Lee, Vikas Vij, Dipanjan Bhadra, Ken Stevens (University of Utah)

Construction of a Timing-Driven Variation-Aware Global Router with Concurrent Multi-Net Congestion Optimization
Radhamanjari Samanta[1], Soumyendu Raha[1], Adil Erzin[2]
[1]Indian Institute of Science (Bangalore), [2]Sobolev Institute of Math. (Russian Academy of Sciences, Novosibirsk, Russia)

3:30 p.m. – 4:00 p.m. Break

4:00 p.m. – 5:30 p.m. Variability and Uncertainty *(Chair: Peng Li, Texas A&M University)*

An Impact of Within-Die Variation on Supply Voltage Dependence of Path Delay
Shinichi Nishizawa, Tohru Ishihara, Hidetoshi Onodera (Kyoto University, Japan)

Impact of Random Telegraph Noise on CMOS Logic Delay Uncertainty
Takashi Matsumoto[1], Kazutoshi Kobayashi[2], Hidetoshi Onodera[1]
[1]Kyoto University (Japan), [2]Kyoto Institute of Technology (Japan)

Multiple Input Switching and Variability-aware Gate Delay Modeling for Ultra-Low Power CMOS Circuits
Prasanjeet Das, Sandeep Gupta (University of Southern California, Los Angeles)

6:30 p.m. – 8:30 p.m. Dinner and Discussion with Past TAU Chairs

Friday, March 29, 2013

8:30 a.m. – 9:00 a.m. Breakfast

9:00 a.m. – 10:30 a.m. Statistical Analysis *(Chair: Debjit Sinha, IBM)*

Eagle-Eye: A Near-Optimal Statistical Framework for Noise Sensor Placement
Tao Wang[1], Chun Zhang[1], Yiyu Shi[1], Jinjun Xiong[2]
[1]Missouri University of Science and Technology, [2]IBM

Speeding up Computation of the max/min of a set of Gaussians for Statistical Timing Analysis and Optimization
Vimitha Kuruvilla[1], Debjit Sinha[1], Jeff Piaget[1], Chandu Visweswariah[1], Nitin Chandrachoodan[2]
[1]IBM, [2]Indian Institute of Technology (Chennai, India)

Probabilistic Standard Cell Modeling Considering Non-Gaussian Parameters and Correlations
André Lange[1], Roland Jancke[1], Joachim Haase[1], Ingolf Lorenz[2], Ulf Schlichtmann[3]
[1]Fraunhofer-Institue for Integrated Circuits, [2]Global Foundries, [3]Technische Universitäat München (Germany)

10:30 a.m. – Closing remarks

11:00 a.m. – 12:00 p.m. Lunch

General Chair: Jinjun Xiong, IBM

Technical Program Committee:
Chirayu Amin, Intel (Chair)
Igor Keller, Cadence
Jaeha Kim, Seoul National University
Kelvin Le, Synopsys
Peng Li, Texas A&M University
Hidetoshi Onodera, Kyoto University
Duaine Pryor, Mentor Graphics
Debjit Sinha, IBM
Tom Spyrou, Altera

Contest Committee:
Debjit Sinha, IBM (Chair)
Luis Guerra e Silva, INESC-ID / IST – TU Lisbon, Portugal
Jia Wang, Illinois Institute of Technology
Shesha Raghunathan, IBM
Dileep Netrabile, IBM
Ahmed Shebaita, Synopsys