Towards a Framework for "Responsible Timing"

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About CLKDA

- Leaders in Variance Analysis – market, technology, expertise
- FX is the first transistor model and simulator specifically engineered for digital variance and delay analysis
- FX Platform is a state of the art distributed static analysis engine
- Variance FX is the leading solution for derate generation
- In production at 28nm, 22nm, 20nm, 16nm, 14nm…

Signoff ownership has changed

- Relationship between foundries, design houses and tool vendors has evolved.
  - Reference flows ≠ ASIC sign-off flows
  - Design houses now own the sign off flow.
  - Foundries only guarantee corners and defect targets, not design specific yield.
- Variability is a significant concern.
- Yield is a significant concern
- But the fiction that old ASIC sign-off flows work persists

Goal for the framework

- Accept that business model of the involved parties not likely to change
  - Foundries deliver good wafers, as defined by defect targets and performance sensors.
  - EDA vendors deliver tools, that must work but not warrantied for a specific purpose
  - Design houses own responsibility for timing sign off, and the yield implications.
- Most important principle is *transparency*
  - Transparency enables all parties to make informed decisions
  - Trust in tools and methods has been retrospective
  - Lack of transparency can break trust
  - Uncertainty in behavior becomes pessimism

What can be measured?

- Performance of devices can be inferred from behavior of oscillators.
- Arrays of devices and metal segments.
- Parametric behavior of all the above across temperature and voltage operating range
- Statistical properties from large samples of all the above
  - Correlated variance (global variables)
  - Uncorrelated variance (local variables)

Not directly measured

- Behavior of cells
- Global corners
  - These are corner process models containing only global variable components
  - These are artificial points in the process space
  - Local variables assumed centered in their distribution for nominal simulation
  - Actual physical devices always have some amount of local variance

Fundamental Question

- How do you define the quality of a STA sign off flow?
- **Objective of STA should be to, as accurately as possible, predict actual silicon performance.**
  - How much slack or any other characteristic a particular STA observes is irrelevant!
  - Timing is not about smiley faces or average slack
  - It is about finding timing exceptions. Finding the problems that will cause your design to fail to yield.

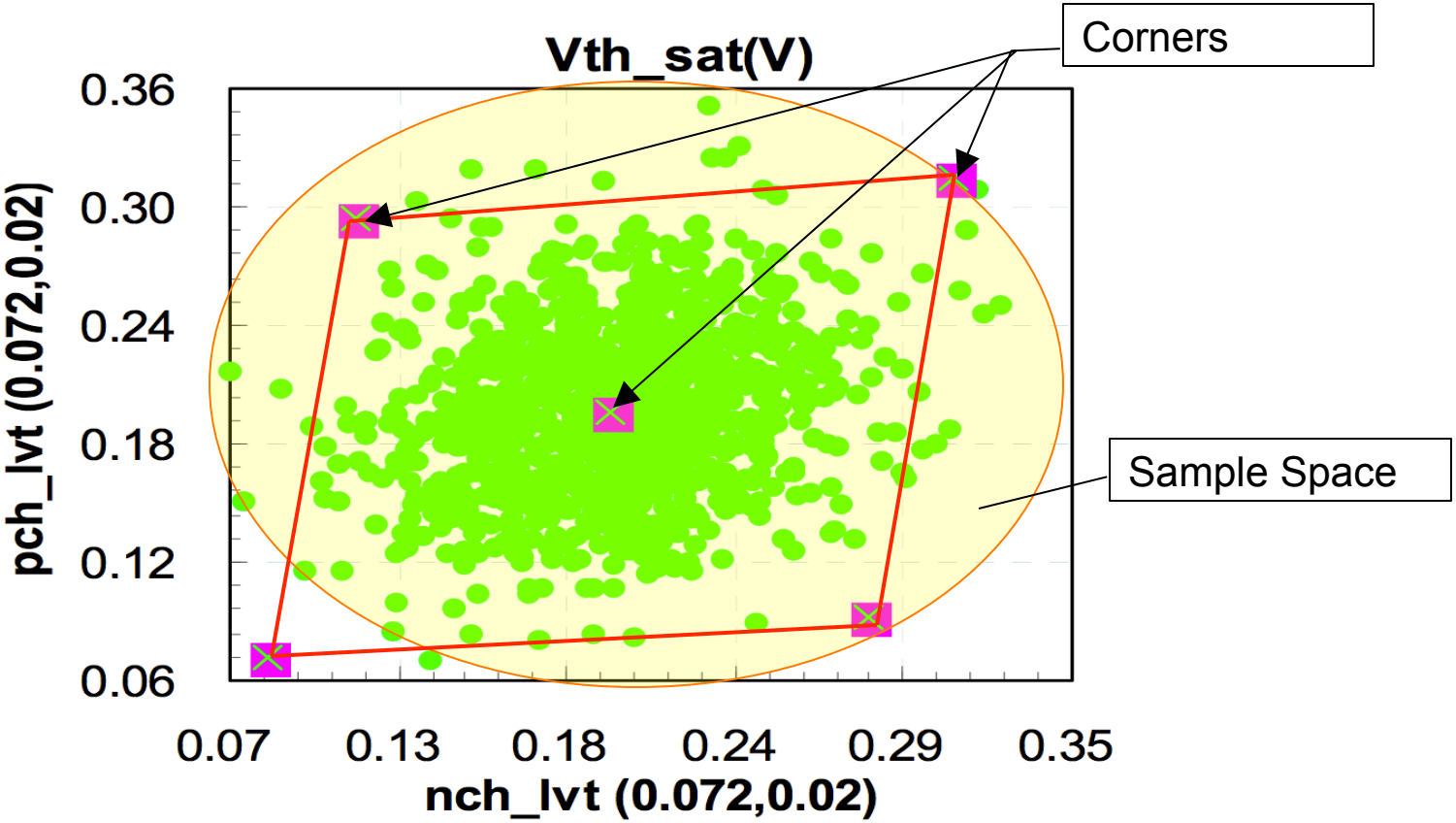
Practicalities

- How do we judge the value of a proposed change to our STA sign-off flows?
  - Derates, constraint uncertainty, changes to SI…
  - Even when in theory they could have a beneficial impact on yield
- Accuracy relative to SPICE
  - Absolute & relative both
  - Completeness of validation circuit
  - Range of validity – temperature, voltage, …
- Cost of creating the data needed to drive the methodology
- Ability of tools to use this data

Clear derivation from SPICE

- Foundries are free to define process models whichever way they want
- EDA vendors are free to implement tools whichever way they want
- However, all basic timing artifacts must be able to trace their behavior to the original SPICE models
  - **STOP** saying you can apply sigma to a total corner!
  - Unless you can justify your math vs. SPICE

Process Space



Global + 3σ vs. Fixed Corners

$$\sigma distance = \frac{abs(corner_{delay} - nominal_{delay})}{\sigma_{delay}}$$

Cell	Corner	Avg σ distance	Max σ Distance	Min σ Distance
Small Inverter	ff	0.75	1.11	0.30
	ss	1.73	2.07	0.72
Large Inverter	ff	2.95	4.52	0.98
	ss	6.85	8.28	2.65
Small Buffer	ff	0.24	1.19	0.002
	ss	0.43	1.77	0.0001
Large Buffer	ff	0.85	4.50	0.001
	ss	1.43	6.81	0.002
Nand	ff	2.43	2.79	1.81
	ss	3.14	3.41	2.11
Mux	ff	0.85	3.82	0.001
	ss	1.75	4.80	0.106

Global vs. Fixed Corner Slew

Cell	Sense	%slew change from ffg to ff
Small inverter	Rise	2.96%
	Fall	1.42%
Large inverter	Rise	2.61%
	Fall	1.60%
Small buffer	Rise	7.69%
	Fall	3.43%
Large buffer	Rise	3.50%
	Fall	2.37%
Nand	Rise	2.51%
	Fall	4.63%
Mux	Rise	4.77%
	Fall	2.76%

Semantic standards

- Currently, the most important STA standards are syntax based
  - SDC
  - Liberty
- Semantics are explicitly left undefined!
  - And are tool specific!
- How can a signoff flow be defined if you can't be sure what the semantics are?
  - You have to (re)validate everything
  - At great expense and cost
  - On every new release

Summary

- Technology, process and responsibilities have evolved
- Sign off flow responsibility now largely in the hands of design houses
- We need to be clear what the purpose timing serves
- Standards in timing are weak and need to evolve
- This is just the beginning