TAU 2014 Program

http://www.tauworkshop.com
March 6 - 7, 2014
Santa Cruz Dream Inn,
Santa Cruz, California, USA

Thursday, March 6, 2014

8:00 a.m. – 8:45 a.m. Breakfast

8:45 a.m. – 9:00 a.m. Opening Remarks

9:00 a.m. – 10:20 a.m. Timing For Analog and Mixed-Signal *(Chair: Vladimir Zolotov, IBM)*

Approximate property checking of mixed-signal circuits
Parijat Mukherjee[1], Chirayu Amin[2], Peng Li[1]
[1]Texas A&M University, [2]Intel

An Exact Linear Time Algorithm for Computing Worst Case Eye Diagrams for a Class of Non-Linear High-Speed Signaling Systems
Aadithya Karthik, Sayak Ray, Robert Brayton and Jaijeet Roychowdhury (UC Berkeley)

Cell-based Physical Design Automation for Analog and Mixed Signal Application
Norihiro Kamae, Islam A.K.M Mahfuzul, Akira Tsuchiya and Hidetoshi Onodera (Kyoto University)

10:20 a.m. – 10:50 a.m. Break

10:50 a.m. – 12:10 p.m. Invited Session *(Chair: Igor Keller, Cadence)*

Horseshoes, Hand Grenades, and Timing Signoff: When Getting Close is 'Good Enough'
Anthony Hill, Arvind Nv and Krishna Panda (Texas Instruments)

Towards a Framework for 'Responsible Timing'
João Geada, (CLK Design Automation)

12:10 p.m. – 1:30 p.m. Lunch

1:30 p.m. – 3:10 p.m. Variability in Timing *(Chair: Tom Spyrou, Altera)*

Increasing the Accuracy of Interconnect Delay Derates: A Path Based Method
Ryan Kinnerk, Colm O'Doherty (Analog Devices), Emanuel Popovici (University College Cork)

Variation Tolerant Design of D-Flip-Flops for Low Voltage Circuit Operation
Shinichi Nishizawa, Tohru Ishihara and Hidetoshi Onodera (Kyoto University)

Modeling Slew Dependent Constraint Arc Variation in Static Timing Analysis
Christian Lütkemeyer and Praveen Ghanta (Broadcom)

Timing Sign-off for Selective Voltage Binning
Vladimir Zolotov, Eric Foreman, Jeffrey Hemmett, Natesan Venkateswaran and Chandramouli Visweswariah (IBM)

3:10 p.m. – 3:30 p.m. Break

3:30 p.m. – 4:30 p.m. Hierarchical Timing *(Chair: Qiuyang Wu, Synopsys)*
Equivalency Checking for Timing Constraints
Subramanyam Sripada, Cho Moon, Loa Mize, Szu-Tsung Cheng and Sonia Singhal (Synopsys)

Sign Off Quality Hierarchical Timing Constraints: Wishful Thinking or Reality?
Oleg Levitsky (Cadence)

4:30 p.m. – 6:00 p.m. Panel: Library Characterization: A Cinderella Story?
Organizer & Moderator: Florin Dartu (TSMC)
Panelists: Federico Politi (Cadence), João Geada (CLK DA), Nanda Gopal (Synopsys), Ramesh Kandadai (Intel), Tom Spyrou (Altera), Jim Dodrill (ARM)

7:00 p.m. – 9:00 p.m. Reception

Friday, March 7, 2014

8:00 a.m. – 8:45 a.m. Breakfast

8:45 a.m. – 9:15 a.m. TAU Timing Contest
Presenter: Jin Hu (IBM)

9:15 a.m. – 10:45 a.m. Testing and Analysis of Analog/Mixed-Signal Circuits *(Chair: Florin Dartu, TSMC)*
Probabilistic Bug Localization for Analog/Mixed-Signal Circuits using Probabilistic Graphical Models
Sangho Youn and Chenjie Gu (Intel)

ABCD-NL: Approximating Non-Linear Analog/Mixed-Signal Systems using Purely Boolean Models for High-speed Simulation and Formal Verification
Aadithya Karthik, Sayak Ray, Pierluigi Nuzzo, Alan Mishchenko, Robert Brayton and Jaijeet Roychowdhury (UCB)

Trace-based fault localization with supply voltage sensor
Miho Ueno, Masanori Hashimoto and Takao Onoye (Osaka University)

10:45 a.m. – 11:00 a.m. Break

11:00 a.m. – 12:10 p.m. Challenges for STA in Advance Process Nodes *(Chair: Christian Lütkemeyer, Broadcom)*
Timing analysis comprehending mask misalignment due to Double Patterning
Arvind Nv and Ajoy Mandal (Texas Instruments)

A Slew/Load-Dependent Approach to Single-Variable Statistical OCV Modeling
Brandon Bautz and Swamy Lokanadham (Cadence)

Challenges in Static Timing Analysis with FinFET
King Ho Tam, Florin Dartu, Tzu-Hen Lin and Tai-Yu Cheng (TSMC)

12:10 p.m. – 12:40 p.m. Lunch

12:40 p.m. – 2:40 p.m. Panel: What's the Next Big Timing Signoff Challenge?
Organizers: Arvind Nv, Anthony Hill, Krishna Panda, Ajoy Mandal (Texas Instruments)
Moderator: Anthony Hill (Texas Instruments)
Panelists: Vladimir Zolotov (IBM), Ruben Molina (Cadence), Hashimoto Masanori (Osaka University), Christian Lütkemeyer (Broadcom), Alireza Kasnavi (Synopsys), Krishna Panda (TI)

General Chair: Chirayu Amin, Intel

Technical Program Committee:
Igor Keller, Cadence (Chair)
Qiuyang Wu, Synopsys
King Ho Tam, TSMC
Masanori Hashimoto, Osaka University
Debjit Sinha, IBM
Tom Spyrou, Altera
Ajoy Mandal, Texas Instruments
Hakan Yalcin, Cadence

Contest Committee:
Jin Hu, IBM (Chair)
Debjit Sinha, IBM
Igor Keller, Cadence

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