TAU 2015 Program

http://www.tauworkshop.com
March 12-13, 2015
Hilton Garden Inn, Monterey, California, USA

Thursday, March 12, 2015

8 a.m. – 8:45 a.m. Breakfast

8:45 a.m. – 9 a.m. Opening Remarks

9 a.m. – 10 a.m. EDA 3.0: EDA As A Service [Keynote] (Chair: Igor Keller, Cadence)
Presenter: Leon Stok (IBM)

10 a.m. – 10:30 a.m. Break

10:30 a.m. – 12:30 p.m. Modeling and optimization (Chair: Florentin Dartu, TSMC)
Re-thinking Polynomial Optimization: Efficient Programming of Reconfigurable Radio Frequency (RF) Systems by Convexification
Fa Wang, Shihui Yin, Minhee Jun, Xin Li, Tamal Mukherjee, Rohit Negi and Larry Pileggi (Carnegie Mellon University)

An Efficient Algorithm for Statistical Timing Yield Optimization
Ramprasath S and Vinita Vasudevan (Indian Institute of Technology, Madras)

*Efficient IC Statistical Modeling and Extraction using a Bayesian Inference Framework**
Li Yu, Ibrahim Elfadel[1] and Duane Boning (MIT, [1]Masdar Institute)

Sparse Circuit Realization of Passive State-Space Linear Models
Jorge Fernandez Villena[1] and Luis Miguel Silveira[2] ([1]Cadence, [2]INESC ID / IST - U. Lisbon)

12:30 p.m. – 2:30 p.m. Lunch and social networking

2:30 p.m. – 4 p.m. Taming constraints, modes, and pessimism in timing (Chair: Tom Spyrou, Altera)
*Taming the Constraints Beast: AutoCons**
Manjeri Krishnan and Brian Borchers (TI)

A Timing Graph Based Approach to Mode Merging
Subramanyam Sripada and Murthy Palla (Synopsys)

A Practical Model to Reduce Margin Pessimism for Multi-Input Switching in Static Timing Analysis of Digital CMOS Circuits
Christian Lütkemeyer (Broadcom)

4 p.m. – 4:30 p.m. Special Topic Session (Chair: Qiuyang Wu, Synopsys)

Strategies for Intellectual Property Protection in Systems Design
Rudolph Darken, Dennis Fernandez and Nelson Rivera (LaRiviere, Grubman PC)

4:30 p.m. – 4:45 p.m. Break

4:45 p.m. – 6 p.m. Panel: Timing analysis in a Mixed Signal World
Organizers: Ruben Molina (Cadence)
Panelists: Ben Farhat (Cadence), Chirayu Amin (Intel), Jacob Rael (Broadcom), Jim Sproch (Synopsys), Yaron Kretchmer (Qualcomm)

7 p.m. – 9 p.m. Reception

Friday, March 13, 2015

8 a.m. – 8:45 a.m. Breakfast

8:45 a.m. – 9 a.m. Opening Remarks

9 a.m. – 9:45 a.m. TAU contest: Incremental Timing Analysis (Chair: Debjit Sinha, IBM)
Presenter: Jin Hu (IBM)

9:45 a.m. – 10 a.m. Break

10 a.m. – 12 p.m. Variability and yield aware timing and noise analysis (Chair: Christian Lütkemeyer, Broadcom)

Statistical Timing Analysis with a Monte Carlo based Framework
Taizhi Liu, Chang-Chih Chen and Linda Milor (Georgia Institute of Technology)

Sharing and Re-Use of Statistical Timing Macro-models across Multiple Voltage Domains
Debjit Sinha, Vladimir Zolotov, Eric Fluhr, Jeffrey Ritzinger, Michael Wood, Natesan Venkateswaran and Stephen Shuma (IBM)

Variation Aware Cross-Talk Aggressor Alignment by Mixed Integer Linear Programming
Vladimir Zolotov[1] and Peter Feldmann[2] ([1]IBM, [2]D E Shaw Research)

*Playing "Texas hold'em" with the yield**
Florentin Dartu and King-Ho Tam (TSMC)

12 p.m. – 1:30 p.m. Lunch and social networking

1:30 p.m. – 3 p.m. Invited session: Challenges for STA in Advance Process Nodes (Chair: Vladimir Zolotov, IBM)

*Static Timing for FPGA devices, Unique Challenges**
Tom Spyrou (Altera)

*Challenges in FPGA Design Timing Closure**
Hong Li, Xin Jin, Yuji Kukimoto and Amit Gupta (Xilinx)

*High-performance and SoC Timing Productivity Challenges**
Andalib Khan, Fritz Rothacker and Kandadai Ramesh (Intel)

3 p.m. – 3:30 p.m. Break

3:30 p.m. – 5 p.m. Panel: Timing constraints: Are they constraining designs or designers?
Organizer: Subramanyam Sripada (Synopsys)
Panelists: Ajay Daga (FishTail Design Automation), Sam Appleton (Ausdia), Qiuyang Wu (Synopsys), Krishna Panda (TI), Bruce Zahn (Intel), Tom Spyrou (Altera)

*Invited papers/abstracts

General Chair: Igor Keller (Cadence)

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