TAU 2015
Monterey, March 12-13

Igor Keller

Debjit Sinha

TAU: Timing Workshop

- STA and related areas
  - Analog circuits … also related
- Right forum for top STA experts
- Covers both mainstream and controversial topics
- Goals:
  - Re-discover STA
  - Bring STA science to design houses, and designer's wisdom to EDA
  - Exchange ideas and build relations
  - Entice students to stay in EDA
  - Nano-vacation (we work so hard!)

Sponsors

- ACM
- Synopsys
- Cadence
- IBM

THANK YOU!

Organization

Organizing Committee

- General chair: Igor Keller (Cadence)
- Technical chair: Debjit Sinha (IBM)
- Contest chair: Jin Hu (IBM)

Contest Committee

- Gregory Schaeffer (IBM)
- Jin Hu (IBM) - Chair
- Vibhor Garg (Cadence)

Technical program committee

- Debjit Sinha (IBM) - **Chair**
- Duaine Pryor (Mentor Graphics)
- Hai Zhou (Northwestern University)
- Hakan Yalcin (Cadence)
- Janet Meiling (Wang) Roveda (University of Arizona)
- Kandadai Ramesh (Intel)
- Ken Stevens (University of Utah)
- King Ho Tam (TSMC)
- Masanori Hashimoto (Osaka University)
- Peng Li (Texas A&M University)
- Qiuyang Wu (Synopsys)
- Tom Spyrou (Altera)
- Xin Li (Carnegie Mellon University)

Technical Program

- ~48 attendees
- EDA, design houses, foundries, academia
  - Altera, IBM, Intel, Cisco, LaRivier, Broadcom, TI, ClkDA, ARM, DE Shaw, TSMC, NVIDIA, Cadence, Synopsys, Ausdia, FishTail DA, Microsemi, Xilinx, Samsung, Qualcomm, NVIDIA
  - 5 universities
- 5 technical sessions
- 1 keynote + 15 papers
- 2 panel discussions
- Timing Contest

Logistics

- Free WiFi
  - Open network: attwifi
- Free parking
- Reception: today 7-9pm
- Slides:
  - Can use your computer if needed
  - Send to ikeller@cadence.com
  - Bring memory stick