Timing constraints: Are they constraining designs or designers?

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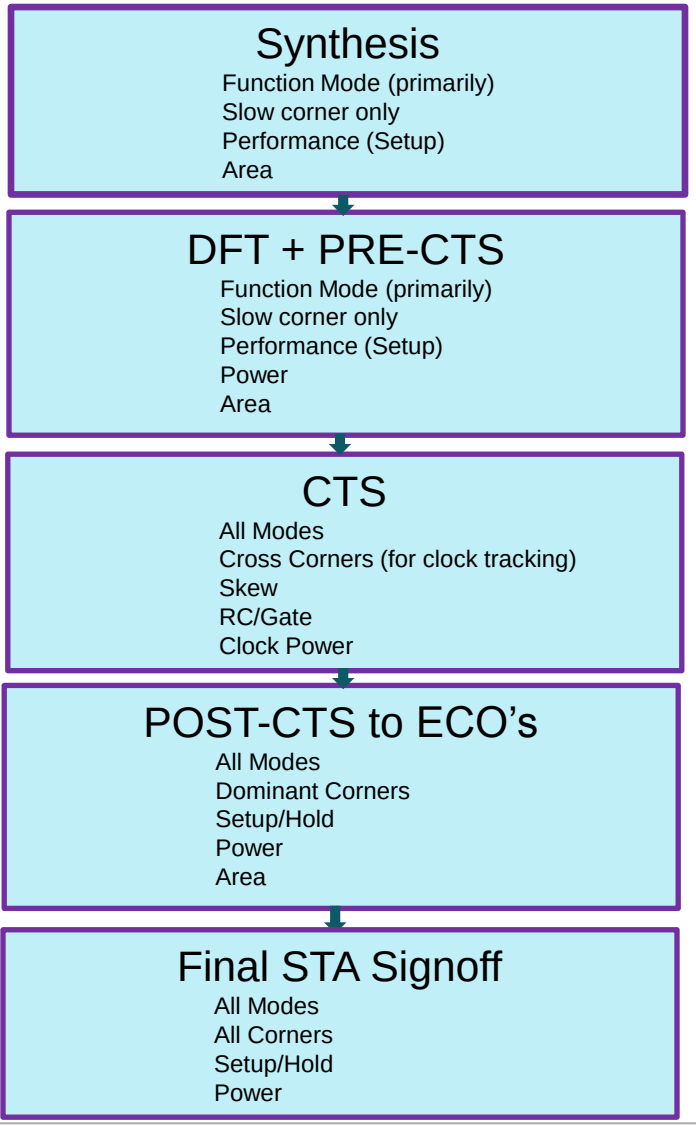
Constraint's For SoC PPA Closure



- Early phase of Implementation Focus on performance and Area
  - No clock tree so hold wont make sense
  - Early power optimization tend to fizzle out during later stages
- CTS Phase Requires all Mode/Corner
  - CTS tool would need to see all clock path's for balancing
  - Cross corner (High/Low temp, Slow/Fast process, Min/Max RC extraction) CTS optimization essential for good quality clock tree
- Later Phase Focus on Hold, Power and Area recovery while keeping Setup clean
  - Need all Modes Function and DFT
  - Need all corner or at least Dominant corners
- Final Signoff
  - Need all Modes Function and DFT
  - Need all corners required for Signoff

What do we need in constraints?

- Be able to constraint PPA goals
  - For Setup Closure
    - Make sure design is timed with correct clock
      - Clocks need to be steered
    - Every path needs to timed at or over required FMAX
      - *Too much over constraining of clock period may be hard to close Setup*
  - For Hold closure
    - Same as setup closure
  - Area/Power
    - Over constraining has adverse effects
- Basically if we are timing every path w/o over constraining too much we are good

Merged vs Multi-Mode constraints?

- Merged Constraints
  - Too many clock definition leads to complexity
    - Have to define Function and DFT clocks
  - Too many Exceptions
    - Eg. Have to add exceptions between DFT and Function paths
  - Not practical at SoC top-level
    - Won't work too many clocks, complex clock steering etc..
- Multi-Mode constraints
  - Explosion of Mode/corner can lead to high resource use
  - Logistical issue's
    - Too many reports/Logs to check
    - Did I miss timing a path
      - Hard to do Setup/Hold coverage analysis
  - Possible gap between Optimization and Signoff
    - Optimization tools choke if run with many Scenario's

Can this be simplified?

- Top-level is almost always Multi-Mode
- Simplified Merged Mode?
  - Constraint written to address specific goals
    - At-speed constraint
    - Scan path constraint
    - Hold path constraint
  - Three set of constraint but each used for specific optimization
    - At-speed constraint focus is on Setup/Area/Power closure
      - Clock steered to cover functional path
    - Scan-path constraint added post DFT to address low-speed scan path
      - Clock steered to cover Scan mode clock
    - Hold constraint covers all paths but not used for performance closure
      - Setup is false.

Contd.

- Will Still need multi-Mode constraint to align with top
  - Most cases simplified constraint can derived from Multi-Mode constraint
- Total scenarios comparison
  - Multi-Mode Method

Modes	Transistor Corner	RC corner	Voltage	Temp	Analysis	Total
FUNC	SS	MAXR, MAXC	Vnom-10%	Low, High	Setup	4
DFT1_SCANSHIFT	SS	MAXC	Vnom-10%	Low	Setup	1
DFT2	SS	MAXR, MAXC	Vnom-10%	Low, High	Setup	4
FUNC	SS,FF	MAXR,MAXC,MINR,MINC	Vnom-10%, Vnom+5%	Low, High	Hold	16
DFT1_SCANSHIFT	SS,FF	MAXR,MAXC,MINR,MINC	Vnom-10%, Vnom+5%	Low, High	Hold	16
DFT2	SS,FF	MAXR,MAXC,MINR,MINC	Vnom-10%, Vnom+5%	Low, High	Hold	16
					Grand Total	**57**

  - Simplified Constraint Method

Modes	Transistor Corner	RC corner	Voltage	Temp	Analysis	Total
At_speed	SS	MAXR, MAXC	Vnom-10%	Low, High	Setup	4
DFT_SCANSHIFT	SS	MAXC	Vnom-10%	Low	Setup	1
Hold	SS,FF	MAXR,MAXC,MINR,MINC	Vnom-10%, Vnom+5%	Low, High	Hold	16
					Grand Total	**21**

Thank You