Sparse Circuit Realization of Passive State-Space Linear Models

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IC designs

- Increasing IC complexity and frequency

- Interconnects play a key role
- Critical impact of EM coupling
Modeling EM effects

- Goal: to extract an equivalent numerical model
Modeling EM effects

- Goal: to extract an equivalent numerical model

- Modeling approach depends on accuracy requirements

![Accuracy vs. Speed Diagram](image-url)
Circuit compatible representation

- **MNA to represent linear circuits as state space systems**
  - Kirchhoff laws with internal variables (states):
    - Voltages at the nodes
    - Currents flowing through inductors and sources

\[
\begin{bmatrix}
G & -F_L^T \\
F_L & 0 \\
\end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix} + \begin{bmatrix} C & 0 \\
0 & L \\
\end{bmatrix} \frac{d}{dt} \begin{bmatrix} v \\ i \end{bmatrix} = \begin{bmatrix} B \\
0 \\
\end{bmatrix} u(t)
\]

\[
y(t) = \begin{bmatrix} B^T & 0 \end{bmatrix} \begin{bmatrix} v \\ i \end{bmatrix}
\]
Simulation and analysis

- Lumped RC for interconnects
Simulation and analysis

- Including parasitics
  - Huge netlists
  - Impact on performance
Model Order Reduction

- **Reduced Order Model**
  - Behavioral equivalent
  - Faster to simulate
Model Order Reduction

- Given the original large-dimensional numerical model

\[
\begin{bmatrix}
C \\
500,000 \times 500,000
\end{bmatrix} \frac{d}{dt} \begin{bmatrix} x \\ 500,000 \times 500,000 \end{bmatrix} + \begin{bmatrix}
G \\
500,000 \times 500,000
\end{bmatrix} \begin{bmatrix} x \\ 500,000 \times 500,000 \end{bmatrix} = \begin{bmatrix} B \end{bmatrix} u(t)
\]

\[y(t) = B^T x\]
Model Order Reduction

• Given the original large-dimensional numerical model

\[
\hat{C} \frac{d}{dt} \begin{bmatrix} \hat{x} \end{bmatrix} + \begin{bmatrix} \hat{G} \end{bmatrix} \begin{bmatrix} \hat{x} \end{bmatrix} = \begin{bmatrix} \hat{B} \end{bmatrix} u(t)
\]

\[
y(t) = \hat{B}^T \hat{x}
\]

• Reduce the dimension of the numerical model
  • At a small cost
  • With I/O equivalent behavior
  • Guarantee certain properties (stability/passivity)
How?

- **Numerical transformations**
  - Matrix projection into a smaller subspace

\[
\begin{align*}
W^T & A V = A_R \\
x & \approx \alpha_0 v_0 + \alpha_1 v_1 + \alpha_2 v_2 + \alpha_3 v_3 + \ldots \\
x & = x(s) \in \mathbb{C}^n \\
\alpha_i & = \alpha_i(s), i = 0 \ldots q - 1
\end{align*}
\]
Numerical transformations

- Matrix projection into a smaller subspace

- Easy to implement and numerically stable/efficient
- Guarantees stability/passivity (orthogonal projection) [1]
- But leads to dense models / hierarchy loss

Back to circuit simulation?

- Now we have a reduced (passive) state space model

\[
\begin{bmatrix}
\hat{C} \\
\hat{G}
\end{bmatrix}
\begin{bmatrix}
\frac{d}{dt} \hat{x} \\
\hat{x}
\end{bmatrix}
+
\begin{bmatrix}
\hat{B}
\end{bmatrix}
u(t)
\]

\[
y(t) = \hat{B}^T \hat{x}
\]

- How to plug back into the simulation?
Back to circuit simulation?

- **Now we have a reduced (passive) state space model**

\[
\begin{align*}
\hat{C} \frac{d}{dt} \begin{bmatrix} \hat{x} \end{bmatrix} + \hat{G} \begin{bmatrix} \hat{x} \end{bmatrix} &= \hat{B} u(t) \\
y(t) &= \hat{B}^T \hat{x}
\end{align*}
\]

- **How to plug back into the simulation?**
  - Electric circuit is the basic EDA format
    - Standard SPICE simulation: positive RLCK elements
    - Number of elements and equations: efficiency
      - Sparsity is an important factor
Nodal Elimination

- Nodal elimination and realizable methods [2,3]
  - Projection = exact or approximate circuit equivalence

Exact:

Approx:

Nodal Elimination

- Nodal elimination and realizable methods (refined) [4,5]
  - Matrix (graph) reordering + local moment matching

Nodal Elimination

- Nodal elimination and realizable methods (refined) [6]
  - Matrix (graph) reordering + local moment matching
  - Sparsity control / minimize fill-in

[6] Ionutiu et al., SPARSE RC. TCAD 2011
Nodal Elimination

- **Nodal elimination and realizable methods**
  - Maintain circuit interpretation and/or sparsity
  - But model density increases with node elimination
  - And difficulty to handle densely coupled systems
  - Needs initial circuit
Transfer Function Realization

- Interpret the reduced order model from input to output

\[ \hat{H}(s) = \hat{B}^T (s\hat{C} + \hat{G})^{-1} \hat{B} \approx H(s) \quad H(s) = \sum_{i=1}^{q} \frac{r_i}{s - p_i} \]

- As a set of poles/zeros [7,8]

[7] Foster’s synthesis
Transfer Function Realization

- Interpret the reduced order model from input to output

\[ \hat{H}(s) = \hat{B}^T (s\hat{C} + \hat{G})^{-1} \hat{B} \approx H(s) \quad H(s) = \sum_{i=1}^{q} \frac{r_i}{s - p_i} \]

- As a set of poles/zeros
  - Each pole/zero as an RLC subcircuit
  - Each I/O is a set of subcircuits connected
    - In parallel if admittance, in series if impedance

![Diagram showing the transfer function realization with RLC subcircuits connected in parallel and series.]
Transfer Function Realization

Interpret the reduced order model from input to output

\[ \hat{H}(s) = \hat{B}^T (s \hat{C} + \hat{G})^{-1} \hat{B} \approx H(s) \quad H(s) = \sum_{i=1}^{q} \frac{r_i}{s - p_i} \]

- No controlled sources
- Independent of original model structure
- Negative RLC elements can appear
Circuit interpretation

• Interpreting the reduced order model

\[
\begin{bmatrix}
\hat{G} \\
\hat{C}
\end{bmatrix} \hat{x} + \frac{d}{dt} \hat{x} = \begin{bmatrix}
\hat{B}
\end{bmatrix} u(t)
\]

• As a set of circuit equations

\[
\hat{c}_{ii} \dot{\hat{x}}_i(t) + \hat{g}_{ii} \ddot{\hat{x}}_i(t) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \dot{\hat{x}}_j(t) + \hat{g}_{ij} \ddot{\hat{x}}_j(t) \right)
\]

• Create a circuit that generates such equations
Controlled Sources Realization

- Using controlled sources [9]

[9] Palenius, TMTT 2004
 Controlled Sources Realization

- Using controlled sources

\[ \ddot{c}_{ii} \ddot{x}_i(t) + \dot{g}_{ii} \dot{x}_i(t) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \ddot{x}_j(t) + \hat{g}_{ij} \dot{x}_j(t) \right) \]
Using controlled sources

Each $x_i$ is a node voltage

\[
\dot{c}_{ii} \dot{x}_i(t) + \dot{g}_{ii} \dot{x}_i(t) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \dot{x}_j(t) + \hat{g}_{ij} \dot{x}_j(t) \right)
\]
Using controlled sources

- Each $x_i$ is a node voltage
- $c_{ii}$ and $g_{ii}$ are grounded capacitors are resistors

\[
\dot{c}_{ii} \dot{x}_i(t) + \dot{g}_{ii} \dot{x}_i(t) = \sum_{k=1}^{m} \hat{b}_{i,k} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \dot{x}_j(t) + \hat{g}_{ij} \dot{x}_j(t) \right)
\]
Controlled Sources Realization

- **Using controlled sources**
  - Each $x_i$ is a node voltage
  - $c_{ii}$ and $g_{ii}$ are grounded capacitors are resistors
  - $b_{ik} c_{ij}$ and $g_{ij}$ are coefficients of controlled sources

\[ \dot{c}_{ii} \ddot{x}_i(t) + \dot{g}_{ii} \dot{x}_i(t) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \dot{x}_j(t) + \hat{g}_{ij} \dot{x}_j(t) \right) \]

![Circuit diagram with controlled sources and node voltages](image)
Controlled Sources Realization

- Using controlled sources
  - General to be applied to any model
  - CS number grow quadratically with model size
  - Non intuitive representation

\[
\begin{align*}
\hat{g}_{ii} & \quad \hat{C}_{ii} \\
\hat{v}_i(t) & \quad b_{il}u_1(t) \\
& \quad b_{im}u_m(t) \\
& \quad \hat{c}_{il}\dot{x}_1(t) + \hat{g}_{il}\dot{x}_1(t) \\
& \quad \hat{c}_{iq}\dot{x}_q(t) + \hat{g}_{iq}\dot{x}_q(t)
\end{align*}
\]
Inverting the MNA stamping procedure

Un stamping

\[
\dot{c}_{ii} \ddot{x}_i(t) + \dot{g}_{ii} \dot{x}_i(t) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t) - \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} \ddot{x}_j(t) + \hat{g}_{ij} \dot{x}_j(t) \right)
\]
UnStamping

- Inverting the MNA stamping procedure

\[- \sum_{j=1, j \neq i}^{q} (\hat{c}_{ij}(\dot{v}_i(t) - \dot{v}_j(t)) + \hat{g}_{ij}(\dot{v}_i(t) - \dot{v}_j(t))) + \dot{v}_i(t) \left( \sum_{j=1}^{q} \hat{c}_{ij} \right) + \dot{v}_i(t) \left( \sum_{j=1}^{q} \hat{g}_{ij} \right) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t)\]
Unstamping

- Inverting the MNA stamping procedure
  - $\Sigma c_{ij}$ and $\Sigma g_{ij}$ are grounded elements from node $i$

\[-\sum_{j=1,j\neq i}^{q} \left( \hat{c}_{ij} (\dot{v}_i(t) - \dot{v}_j(t)) + \hat{g}_{ij} (\dot{v}_i(t) - \dot{v}_j(t)) \right) + \dot{v}_i(t) \left( \sum_{j=1}^{q} \hat{c}_{ij} \right) + \dot{v}_i(t) \left( \sum_{j=1}^{q} \hat{g}_{ij} \right) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t)\]
Unstamping

- Inverting the MNA stamping procedure
  - $\Sigma c_{ij}$ and $\Sigma g_{ij}$ are grounded elements from node $i$
  - $b_{ik}$ are controlled sources from I/O $k$ to node $i$

\[
\begin{align*}
- \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij} (\dot{v}_i(t) - \dot{v}_j(t)) + \hat{g}_{ij} (\hat{v}_i(t) - \hat{v}_j(t)) \right) + \\
\hat{v}_i(t) \left( \sum_{j=1}^{q} \hat{c}_{ij} \right) + \hat{v}_i(t) \left( \sum_{j=1}^{q} \hat{g}_{ij} \right) &= \sum_{k=1}^{m} \hat{b}_{ik} u_k(t)
\end{align*}
\]
Unstamping

• Inverting the MNA stamping procedure
  • $\Sigma c_{ij}$ and $\Sigma g_{ij}$ are grounded elements from node $i$
  • $b_{ik}$ are controlled sources from I/O $k$ to node $i$
  • $-c_{ij}$ and $-g_{ij}$ are capacitors and resistors between nodes $ij$

\[- \sum_{j=1, j \neq i}^{q} \left( \hat{c}_{ij}(\dot{v}_i(t) - \dot{v}_j(t)) + \hat{g}_{ij}(\dot{v}_i(t) - \dot{v}_j(t)) \right) +
\hat{v}_i(t) \left( \sum_{j=1}^{q} \hat{c}_{ij} \right) + \hat{v}_i(t) \left( \sum_{j=1}^{q} \hat{g}_{ij} \right) = \sum_{k=1}^{m} \hat{b}_{ik} u_k(t)\]
Inverting the MNA stamping procedure

Generates negative elements during unstamping
- Model still passive, inner elements not physical
- 2q controlled sources per external port
Unstamping: block structure preserving

- **Inverting MNA stamping procedure** [10]
  - Keep original MNA variable hierarchy (Split projector)

\[
\begin{bmatrix}
\hat{G} & -\hat{F}_L^T \\
\hat{F}_L & 0
\end{bmatrix}
\begin{bmatrix}
\dot{\hat{v}} \\
\hat{i}
\end{bmatrix} +
\begin{bmatrix}
\hat{C} & 0 \\
0 & \hat{L}
\end{bmatrix}
\frac{d}{dt}
\begin{bmatrix}
\hat{v} \\
\hat{i}
\end{bmatrix} =
\begin{bmatrix}
\hat{B} \\
0
\end{bmatrix} u(t)
\]
Unstamping: block structure preserving

- **Inverting MNA stamping procedure**
  - Rewrite as second order system

\[
\begin{align*}
\begin{pmatrix}
\hat{C} \\
\hat{G}
\end{pmatrix} + \frac{1}{s} \begin{pmatrix}
\hat{F}_L^T \\
\hat{L} \\
\hat{F}_L
\end{pmatrix} \dot{v} &= \begin{pmatrix}
\hat{B}
\end{pmatrix} u(t)
\end{align*}
\]
Unstamping: block structure preserving

- **Inverting MNA stamping procedure**
  - Rewrite as second order system
    \[
    \left( \begin{bmatrix} \hat{C} \end{bmatrix}_S + \begin{bmatrix} \hat{G} \end{bmatrix}_S + \frac{1}{S} \begin{bmatrix} \hat{F}_L^T \hat{L}^{-1} \hat{F}_L \end{bmatrix}_S \right) \hat{v} = \begin{bmatrix} \hat{B} \end{bmatrix} u(t)
    \]
  - Keep I/O nodes unreduced: avoids controlled sources
  - Direct interpretation of the variables: negative entries
  - Diagonalize inductive part to avoid loops

![Diagram of electric circuit](image)
Unstamping: diagonalization

- **Inverting MNA stamping procedure [11]**
  - Apply coordinate transformation/diagonalization

\[
\left( [\Delta_c^s + I + \frac{1}{s}K] \right) \bar{v} = [\bar{B}] u(t)
\]

Unstamping: diagonalization

- **Inverting MNA stamping procedure**
  - Apply coordinate transformation/diagonalization
  
  \[
  \left( \left[ \Delta_C \right] s + \left[ I \right] + \frac{1}{s} \left[ K \right] \right) \bar{v} = \left[ B \right] u(t)
  \]

  - Diagonal matrices for capacitors and resistors
  - Inverse of K: grounded and mutual inductors
  - All positive RLC, but 2q controlled sources per port
Proposed Realization Approach

- Minimize the number of controlled sources
- Guarantee positivity of RLC elements
- Increase sparsity ratio / minimize coupling
- Be general: independent on structure of initial model
Proposed Realization Approach

- **We borrow from transfer function realization**
  - Form the model in I/O admittance form

\[ \hat{H}(s) = \hat{B}^T (s\hat{C} + \hat{G})^{-1} \hat{B} = Y(s) \]
Proposed Realization Approach

- We borrow from transfer function realization
  - Form the model in I/O admittance form
- Diagonalize the (semi-definite positive) system matrices
  - Solve eigenvalue problem and apply transformation

\[
(s \bar{C} + \bar{G}) x = \bar{B} u, \quad y = \bar{E} x.
\]
Proposed Realization Approach

- For each I/O response, we have a SISO problem

\[(s\bar{C} + \bar{G}) x = bu, \quad y = ex.\]
Proposed Realization Approach

- For each I/O response, we have a SISO problem

\[(s\Delta_d + \Delta_s)x = 1^n u, \quad y = 1^T x.\]

- Scale the diagonal matrices with b and e
Proposed Realization Approach

- For each I/O response, we have a SISO problem
  \[ (s\Delta_d + \Delta_s) x = \bar{1}u, \quad y = \bar{1}^T x. \]
  - Each equation: frequency dependent admittance
  - Can be represented as a simple RLC subcircuit
  - Real entries: series RL
    \[ Y_k(s) = \frac{1}{a + sc} \]
  - Complex entries (conjugate pairs): RLC circuit
    \[ Y_k(s) = \frac{1}{(a+jb)+s(c+jd)} + \frac{1}{(a-jb)+s(c-jd)} \]
For each I/O response, we have a SISO problem

\[ i(s) = \sum_{k=0}^{q} Y_k(s)v(s) \]

- Each equation: frequency dependent admittance
- Can be represented as a simple RLC subcircuit
- Total I/O response: sum of admittances
- Parallel connection of admittances

**Proposed Realization Approach**
Proposed Realization Approach

- For each I/O response, we have a SISO problem
  \[ Y_k(s) = Y_k^+(s) - Y_k^-(s) \]

- To avoid negative elements
  - Split each sub-circuit into positive and negative parts

\[ i(s) = \sum_{k=0}^{q} Y_k^+(s)u(s) - \sum_{k=0}^{q} Y_k^-(s)u(s) \]

\[ Y^+(s) = \frac{n_1^+ + sn_2^+}{(a^2+b^2)+s(2ac+2bd)+s^2(c^2+d^2)} \]
\[ Y^-(s) = \frac{n_1^- + sn_2^-}{(a^2+b^2)+s(2ac+2bd)+s^2(c^2+d^2)} \]
Proposed Realization Approach

- For each I/O response, we have a SISO problem
  \[ Y_k(s) = Y_k^+(s) - Y_k^-(s) \]

- To avoid negative elements
  - Split each sub-circuit into positive and negative parts

\[ i(s) = \sum_{k=0}^{q} Y_k^+(s)v(s) - \sum_{k=0}^{q} Y_k^-(s)v(s) \]
Proposed Realization Approach

- For each I/O response, we have a SISO problem
  - Real poles and zeros: series RL
  - Complex conjugate pairs: different RLGÇ nets

\[
Y_{RLGC}(s) = \frac{G+sc}{(1+GR)+s(RC+GL)+s^2(LC)}
\]
Proposed Realization Approach

- From the SISO model to general MIMO?
Proposed Realization Approach

- From the SISO model to general MIMO
  - MIMO transfer function is a matrix

\[
Y = \begin{bmatrix}
  Y_{11} & \cdots & Y_{1m} \\
  \vdots & \ddots & \vdots \\
  Y_{m1} & \cdots & Y_{mm}
\end{bmatrix}
\]
Proposed Realization Approach

• From the SISO model to general MIMO
  • MIMO transfer function is a matrix
    \[ Y = \begin{bmatrix} Y_{11} & \cdots & Y_{1m} \\ \vdots & \ddots & \vdots \\ Y_{m1} & \cdots & Y_{mm} \end{bmatrix} \]
  • Each entry is an individual SISO transfer function
  • We can apply admittance unstamping
  • E.g., for a 2-port system
    \[
    i_1 = (Y_{11} + Y_{12})v_1 - Y_{12}(v_1 - v_2) \\
    i_2 = (Y_{22} + Y_{12})v_2 - Y_{12}(v_2 - v_1)
    \]
Proposed Realization Approach

- From the SISO model to general MIMO
  - MIMO transfer function is a matrix
  - We can apply admittance unstamping

\[
\begin{align*}
i_1 &= (Y_{11} + Y_{12})v_1 - Y_{12}(v_1 - v_2) \\
i_2 &= (Y_{22} + Y_{12})v_2 - Y_{12}(v_2 - v_1)
\end{align*}
\]
Proposed Realization Approach

- From the SISO model to general MIMO
  - MIMO transfer function is a matrix
Proposed Realization Approach

• From the SISO model to general MIMO
  • MIMO transfer function is a matrix
Proposed Realization Approach

• **Pros**
  • Only algebraic transformations:
    • Keeps accuracy and system properties
  • Does not depend on the original system structure
  • Very sparse positive realization
  • Only positive RLC elements, no coupling
  • 1 voltage controlled voltage source (fixed value) per port
  • Intuitive circuit representation: poles and zeros
  • Allows for further compression depending on frequency

• **Cons**
  • Number of sub-circuits grows with number of ports
  • Suitable for systems with small number of ports
Numerical Results

- **Generic models**: RL, LC, PEEC based, Macro-modeling

<table>
<thead>
<tr>
<th>Benchmark</th>
<th>Model</th>
<th>Freq. (GHz)</th>
<th>Ports</th>
<th>Original states</th>
<th>ROM states</th>
<th>Y-Sparse nodes</th>
<th>R</th>
<th>C</th>
<th>L</th>
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<tr>
<td>On-chip spiral [6]</td>
<td>PEEC (RL)</td>
<td>0-60</td>
<td>1</td>
<td>1434</td>
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<td>-</td>
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Numerical Results

- **Generic models: RL, LC, PEEC based, Macro-modeling**

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- Keeps accuracy
Numerical Results

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<th>Original states</th>
<th>ROM states</th>
<th>Y-Sparse nodes</th>
<th>R</th>
<th>C</th>
<th>L</th>
<th>CS</th>
</tr>
</thead>
<tbody>
<tr>
<td>On-chip spiral [6]</td>
<td>PEEC (RL)</td>
<td>0-60</td>
<td>1</td>
<td>1434</td>
<td>14</td>
<td>15</td>
<td>14</td>
<td>0</td>
<td>14</td>
<td>0</td>
</tr>
<tr>
<td>3-D EM problem [12]</td>
<td>PEEC (LC)</td>
<td>0.001-5</td>
<td>1</td>
<td>305</td>
<td>35</td>
<td>36</td>
<td>0</td>
<td>35</td>
<td>35</td>
<td>1</td>
</tr>
<tr>
<td>3-D Connector [19]</td>
<td>PEEC</td>
<td>0.001-10</td>
<td>6</td>
<td>256</td>
<td>91</td>
<td>2157</td>
<td>1687</td>
<td>1000</td>
<td>1583</td>
<td>6</td>
</tr>
<tr>
<td>S-parameter [13]</td>
<td>SysId</td>
<td>1-10</td>
<td>2</td>
<td>-</td>
<td>42</td>
<td>187</td>
<td>128</td>
<td>111</td>
<td>123</td>
<td>6</td>
</tr>
<tr>
<td>H Clock Tree</td>
<td>PEEC</td>
<td>0.1-100</td>
<td>17</td>
<td>3543</td>
<td>90</td>
<td>16008</td>
<td>12676</td>
<td>8225</td>
<td>11003</td>
<td>17</td>
</tr>
</tbody>
</table>

- Less favorable case: H-clock tree with 17 ports
  - Nodes: 2014 to 16008 (8x)
  - Resistors: 1564 to 12676 (8x)
  - Capacitors: 2295 to 8225 (4x)
  - Inductors: 1530 to 11003 (7x)
  - Mutual Inductors: 215985 to 0
Numerical Results

- **H-clock tree**
  - Still has smaller number of non-zeros
Conclusions and future lines

• **A circuit synthesis approach for state-space models**
  • Generates sparse netlists with only positive RLC
    • From any passive state-space model
  • Minimizes number of controlled sources
  • Works better for
    • systems with complex response
    • And small I/O count

• **Open challenges**
  • Parameterized models: handle physical parameters?
  • Reduce the number of controlled sources?
  • Reduce the number of subnets for large I/O count?
Acknowledgements

• Work partially supported by Portuguese national funds through **FCT, Fundação para a Ciência e a Tecnologia**, under projects

  • PTDC/EEI-ELC/3002/2012
  • PEst-OE/EEI/LA0021/2013