



CALL FOR PAPERS – TAU 2016

ACM International Workshop on Timing Issues in the
Specification and Synthesis of Digital Systems
Mar 10-11, 2016 – Bay area, CA – www.tauworkshop.com



It has become clear that timing analysis is NO longer a solved problem. So, what are new challenges as the industry embraces 14/10nm and below, rides the wave of ultra-low-power mobile, wearable devices and jumps on the “Internet of Things” (IoT) bandwagon? How to meet the insatiable demands for accuracy, performance, capacity and functionality? How are multi-core and multi-machine helping? Or is it time to move onto higher levels of abstraction? What about more fundamental challenges coming from process physics, 3D, variability, voltage scaling, analog effects, mixed signal modeling and validation?

The TAU series of workshops provide an informal forum for practitioners and researchers working on these and other temporal aspects of analog and digital systems to disseminate early work and engage in a free discussion of ideas. The twenty-third in the TAU series, the **TAU 2016** workshop invites submissions and proposals from the traditional as well as emerging areas related to the timing properties of digital electronic systems, including but not limited to the topics listed below.

Timing (including incremental timing)

- System/circuit-level timing
- Gate/transistor-level timing
- Timing of mixed signal circuits, FPGAs
- New types of latches, dual-edge devices, etc.
- Distributed timing analysis

Variability

- Timing analysis under variation and uncertainty
- Ultra-low voltage induced variation effects
- Statistical timing analysis and optimization
- Sensitivity/criticality analysis
- Yield analysis and optimization

Signal integrity

- Crosstalk modeling, analysis, avoidance and optimization
- Noise and glitch analysis
- Variation-aware signal integrity analysis

Characterization

- Cell (library) characterization
- Variation effects and corner reductions
- Latch characterization
- Simulation and characterization of SRAM circuits

Emerging technologies

- Full custom design analysis
- Smart sensor placement
- Timing issues for 3D ICs, TSVs
- Timing implications of emerging technologies

Modeling and simulation

- Transistor level modeling
- Analog circuit modeling
- Circuit level simulation
- Delay models and metrics
- Aging, reliability modeling and simulation

Power, trade-offs and optimization

- Timing issues in low-power design
- Power-delay tradeoffs
- Timing driven layout optimization
- Timing driven synthesis, re-synthesis
- Circuit optimization

Clocking

- Complex clock trees and networks
- Clocking, synchronization, and skew
- Clock domains, static/dynamic logic
- Novel clocking schemes

Hierarchical timing

- Macro-modeling: timing, SI, power, etc.
- Hierarchical optimization and signoff
- Integration/Interoperation with implementation flow

Others

- Integrated functional-temporal analysis
- Formal theories and methods
- Asynchronous systems
- Localization and debug of timing errors

DATES

Paper submission deadline (extended):
~~November 20,~~
November 25,
2015

Acceptance notification:

December 23, 2015

Camera ready papers due:

January 8, 2016

Contest registration starts:

October 1, 2015

Early binary due:

February 1, 2016

Final binary due:

February 15, 2016

ORGANIZATION

General chair:
Debjit Sinha (IBM)

Technical program chair:
Qiuyang Wu
(Synopsys)

Past chair: Igor Keller (Cadence)

Contest chair:
Jin Hu (IBM)

Timing contest: Similar to prior years, TAU is organizing a timing contest. The topic for the TAU 2016 contest is “Timing macro-modeling”. Details are posted on the workshop website. Winners of the contest will be awarded plaques as well as cash prizes!

SUBMISSION OF PAPERS

All papers must be submitted electronically via the workshop website www.tauworkshop.com. Submissions are limited to 8 pages in the double column proceedings format. In order to allow for a blind review, submitted pdf version of the papers should not contain the authors’ name or any direct reference to the authors. TAU is a workshop aimed at fostering a high level of professional interaction, not a conference. Copies of papers will be provided to the attendees, but the proceedings will not be published by the ACM or the IEEE. *Therefore, accepted papers can still be submitted to other conferences and journals (e.g. DAC 2016).*