TAU 2016 Program

http://www.tauworkshop.com
March 10-11, 2016
Hilton Sonoma Wine Country, Santa Rosa, California, USA

Thursday, March 10, 2016

8 – 8:45 a.m. Breakfast

8:45 – 9 a.m. Opening Remarks from general chair

9 – 9:45 a.m. Optimizing Automotive Drive Trains: from Energy Source to where the Rubber Meets the Road [Keynote] (Chair: Debjit Sinha, IBM)
Speaker: Patrick Groeneveld (Synopsys)

9:45 – 10:15 a.m. Break

10:15 – 11:05 a.m. Interconnect Modeling and Optimization (Chair: Igor Keller, Cadence)

1. *Layer-to-Layer Interconnect Variation is a Significant but Unmodeled Source of Hold Time Optimism in Conventional BEOL Corner Models*
   Christian Lutkemeyer, Ali Anvar (Broadcom)

2. *Accurate Timing Updates for Circuit Optimization without Explicit Parasitic Data*
   Ruiming Li, Rajendran Panda, Tong Xiao, Ted Hong, Xiaomi Mao (Oracle)

3. *Comparison of channel protocols for low latency, low energy communication over transmission lines*
   Shomit Das, Kenneth Stevens (University of Utah)

11:10 a.m. – 12 p.m. Design Reliability (Chair: Oscar Ou, MediaTek)

1. *Mitigation of NBTI-induced Timing Degradation in Processor*
   Song Bian, Michihiro Shintani, Zheng Wang, Masayuki Hiromoto, Anupam Chattopadhyay and Takashi Sato (Kyoto University, Nanyang Technological University)

2. *Measurement of Timing Error Detection Performance of Software-based Error Detection Mechanisms and Its Correlation with Simulation*
   Yutaka Masuda, Masanori Hashimoto, Takao Onoye (Osaka University)

3. *Transistor Size Optimization Methodology for Logic Circuits Considering Variations caused by BTI and Process*
   Michitarou Yabuuchi, Kazutoshi Kobayashi (Kyoto Institute of Technology)

12 – 2 p.m. Lunch and social networking

2 – 2:45 p.m. Timing in Biologic Systems [Special session invited talk] (Chair: Vladimir Zolotov, IBM)
Speaker: Louis Scheffer (Howard Hughes Medical Institute, USA)

2:45 – 4:15 p.m. Design Variation and Statistical Analysis (Chair: Tom Spyrou, Altera/Intel)

1. *Statistical Path Tracing in Timing Graphs*
   Vasant Rao, Debjit Sinha, Nitin Srimal and Prabhat Maurya (IBM)

2. *Efficient Transistor-level Timing Yield Estimation via Line Sampling*
   Hiromitsu Awano and Takashi Sato (Kyoto University)

3. *Generation and Use of Statistical Timing Macro-models considering Slew and Load Variability*
   Debjit Sinha, Vladimir Zolotov, Jin Hu, Sheshashayee Raghunathan, Adil Bhanji and Christine Casey (IBM)

4. *Importance of Modeling Non-Gaussianities in Static Timing Analysis in sub-16nm Technologies*
   Praveen Ghanta, Igor Keller (Cadence)

5. *Practical Statistical Static Timing Analysis with Current Source Models*
   Debjit Sinha, Vladimir Zolotov, Sheshashayee Raghunathan, Michael Wood and Kerim Kalafala (IBM)

4:15 – 4:30 p.m. Break

4:30 – 6:00 p.m. Panel: Can we still have, or even need, timing interoperability in the age of EDA silos?
Organizer: Joao Geada (CLK DA)
Panelists: Jim Sproch (Synopsys), Florin Dartu (TSMC), Ruben Molina (Cadence), Vasant Rao (IBM), Paul Penzes (Qualcomm)

7 – 9 p.m. Reception

Friday, March 11, 2016

8 – 8:45 a.m. Breakfast

8:45 – 9 a.m. Opening Remarks from technical program chair

9 – 9:45 a.m. In Search of Lost Time (Chair: Qiuyang Wu, Synopsys)
Speaker: Andrew B. Kahng (Departments of CSE and ECE, University of California, San Diego)

9:45 – 10:30 a.m. TAU contest: Timing macro-modeling (Chair: Qiuyang Wu, Synopsys)
Presenters: Jin Hu (IBM), Song Chen (Synopsys)

10:30 – 10:45 a.m. Break

10:45 a.m. – 12:15 p.m. Advances in Timing Analysis (Chair: Richard Phillips - nVidia)
1. *Integrating a Hierarchical Timing Flow into an Advanced Timing Closure System*
   Yazdan Aghaghiri, Richard Phillips, Lane Albanese (nVidia)

2. *A Distributed Timing Analysis Framework for Large Designs*
   Tsung-Wei Huang, Martin Wong, Debjit Sinha, Kerim Kalafala, Natesan Venkateswaran (IBM)

3. *An efficient methodology for model extraction using waveform analysis*
   Sneh Saurabh, Naresh Kumar (Cadence)

4. *Mode Merging: Identification of Mergeable Modes*
   Subramanyam Sripada, Murthy Palla (Synopsys)

5. *High Performance Latch Based Design: Optimization and Timing Verification Challenges**
   Kumar Subramanian, K.S. Ramesh (Intel)

12:15 – 2 p.m. Lunch and social networking

2 – 3:15 p.m. Timing of FPGAs and Asynchronous Designs (Chair: Hong Li - Xilinx)

1. *The Stratix 10 Hyperflex Architecture and its impact on Timing Analysis**
   Tom Spyrou (Altera/Intel)

2. *Highly-dense Mixed Grained Reconfigurable Architecture with Via-switch*
   Junshi Hotate, Takashi Kishimoto, Toshiki Higashi, Hiroyuki Ochi, Ryutaro Doi, Munehiro Tada, Tadahiko Sugibayashi, Kazutoshi Wakabayashi, Hidetoshi Onodera, Yukio Mitsuyama and Masanori Hashimoto (Osaka University, Ritsumeikan University, NEC, Kyoto University, Kochi University of Technology, JST, CREST)

3. *A Practical Approach to Clock Skew Optimization for FPGAs**
   Atul Srinivasan (Xilinx)

4. *Relative Placement in Timed Asynchronous Design*
   Tannu Sharma, William Lee and Kenneth Stevens (University of Utah)

3:15 – 3:30 p.m. Break

3:30 – 5 p.m. Panel: How low can we go? Challenges when designing at ultra-low voltage
Organizer: Florin Dartu (TSMC)
Panelists: TBA

*Invited papers/abstracts

TAU sponsors: