Practical Statistical Static Timing Analysis with Current Source Models

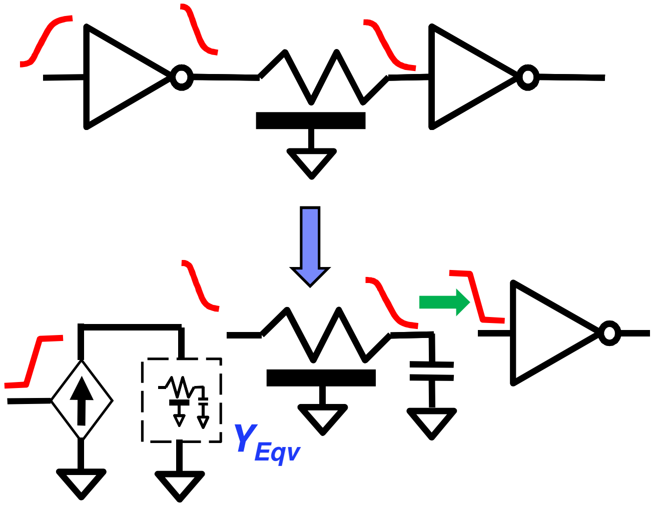
Debjit Sinha, Vladimir Zolotov[1], Sheshashayee K. Raghunathan[2], Michael H. Wood, Kerim Kalafala

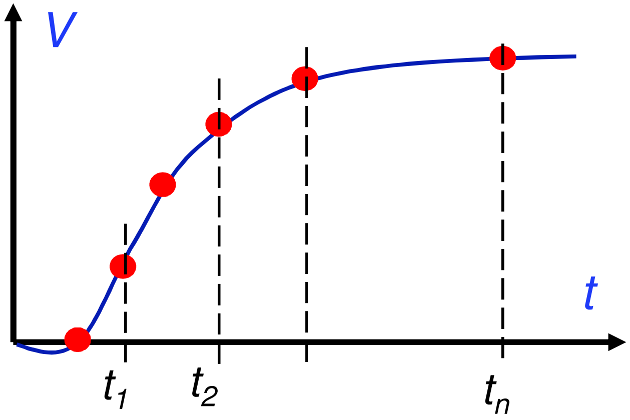
IBM Systems, Poughkeepsie, USA
IBM Thomas J. Watson Research, Yorktown Heights, USA[1]
IBM Systems, Bangalore, India[2]

{dsinha, zolotov, woodm, kalafala}@us.ibm.com; shesha.raghunathan@in.ibm.com

Driver and Signal Modeling

- ***Delay/Slew/Ceff* driver model is too inaccurate**
- **Current Source Model (CSM) has better accuracy**
  - Einstimer uses efficient implementation based on dynamic effective capacitance
    - *P Feldmann, S Abbaspour, D Sinha, et al., Driver waveform computation for timing analysis with multiple voltage threshold driver models, DAC 2008*
- **Waveforms model is necessary companion**
  - Better accuracy but higher computational cost and memory footprint
- **Einstimer implements statistical timing**
  - Delays, slews, ATs, RATs, etc. are modeled with linear or bilinear forms
    - Cross-terms model interaction of sources of variations like dependence of variability on Vdd





$$t = t_0 + \overbrace{t_V \Delta V + t_1 \Delta X_1 + \ldots + t_R \Delta R_a}^{\text{Linear terms}} + \overbrace{t_{V,1} \Delta V \Delta X_1 + \cdots + t_{V,R} \Delta V \Delta R_a}^{\text{Cross-terms}}$$

Efficient statistical model of waveform is needed

Statistical waveform models

- **Time points are modeled with statistical canonical form**
  - ***H.Fatemi, S.Nazarian, and M.Pedram, "Statistical logic cell delay analysis using a current-based model, DAC2006***
  - High memory consumption and redundancy
    - Time moments are highly correlated
- **Statistical waveform model approximates variability with timing shift and scale**

$$V(t) = V_{nom}\left(t - S[t - t_0] - D\right)$$

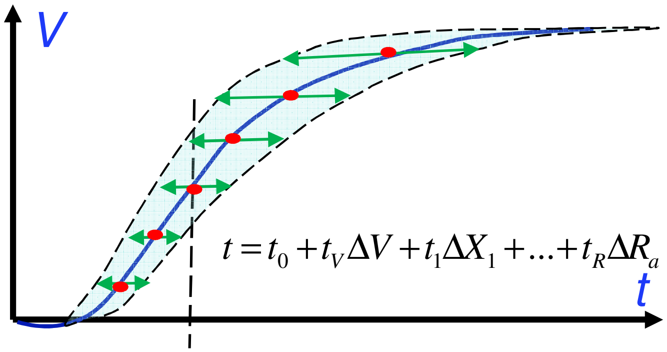
  - Nominal waveform $V_{nom}(t)$ defines shape
  - Canonical form of shift acts as statistical delay

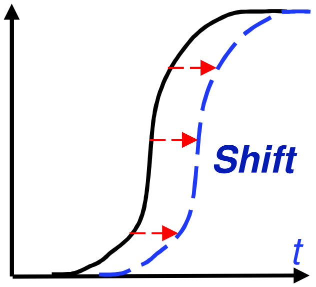
$$D = d_0 + s_V \Delta V + d_1 \Delta X_1 + ... + d_R \Delta R_a$$

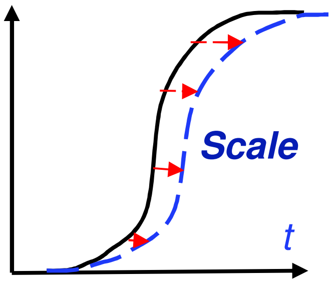
  - Canonical form of scale acts as statistical slew

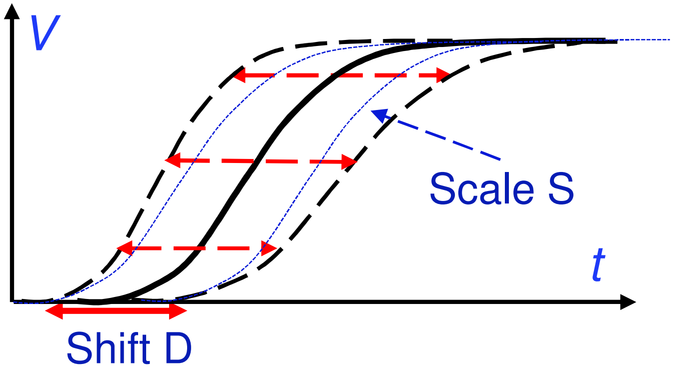
$$S = s_0 + s_V \Delta V + s_1 \Delta X_1 + ... + s_R \Delta R_a$$

    - ***V. Zolotov, J. Xiong, C. Visweswariah, S. Abbaspour , D. Hathaway, "Compact modeling of variational waveforms", ICCAD 2007 computes sensitivities by solving CSM differential equations, which is rather inefficient.***
- **Efficient technique for computing and propagating statistical waveform is needed**
  - Support incremental timing





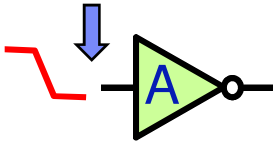


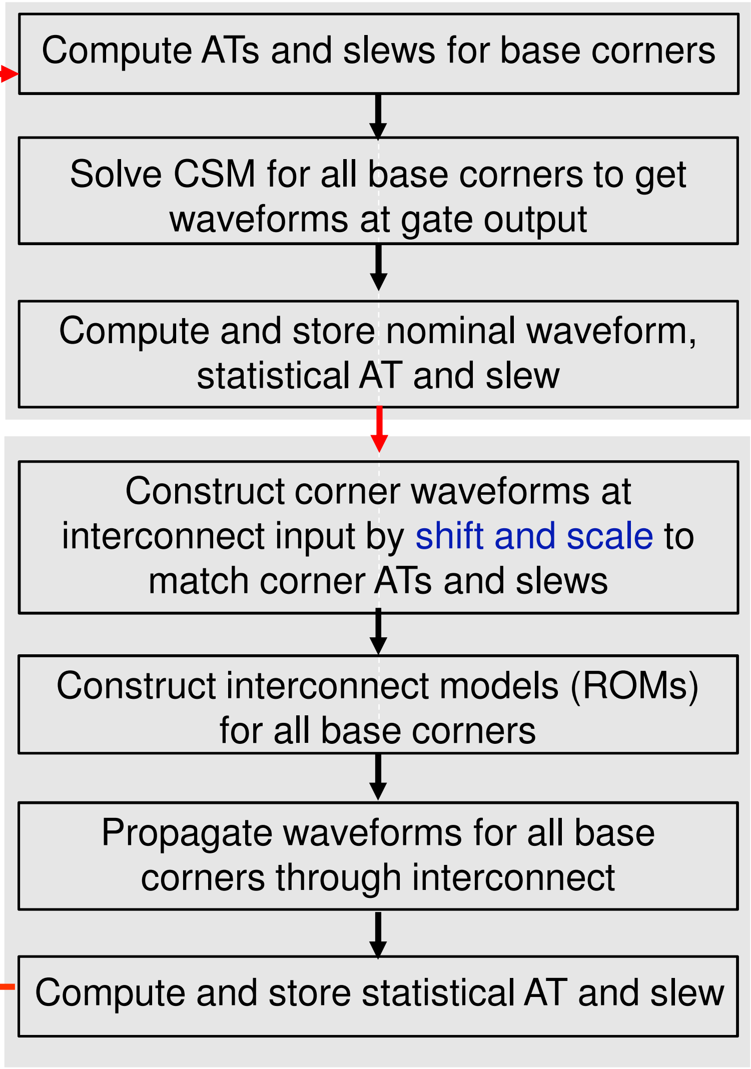


Statistical waveform propagation ("Partial CSM")

Statistical AT & slew at gate input

$S = s_0 + s_V \Delta V + \ldots + s_R \Delta R_a$





Compute ATs and slews for base corners

Solve CSM for all base corners to get waveforms at gate output

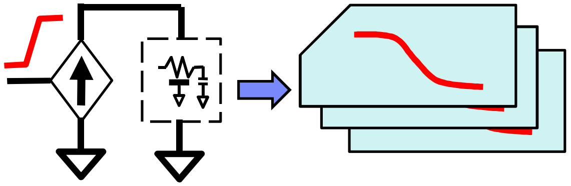
Compute and store nominal waveform, statistical AT and slew

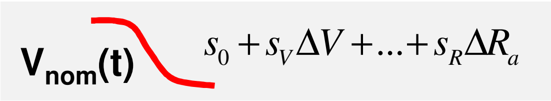
Construct corner waveforms at interconnect input by shift and scale to match corner ATs and slews

Construct interconnect models (ROMs) for all base corners

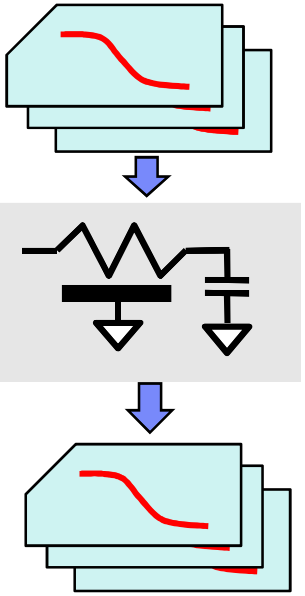
Propagate waveforms for all base corners through interconnect

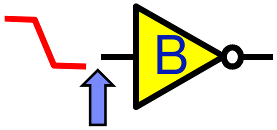
Compute and store statistical AT and slew





$V_{nom}(t)$ $s_0 + s_V \Delta V + \ldots + s_R \Delta R_a$





$S = s_0 + s_V \Delta V + \ldots + s_R \Delta R_a$

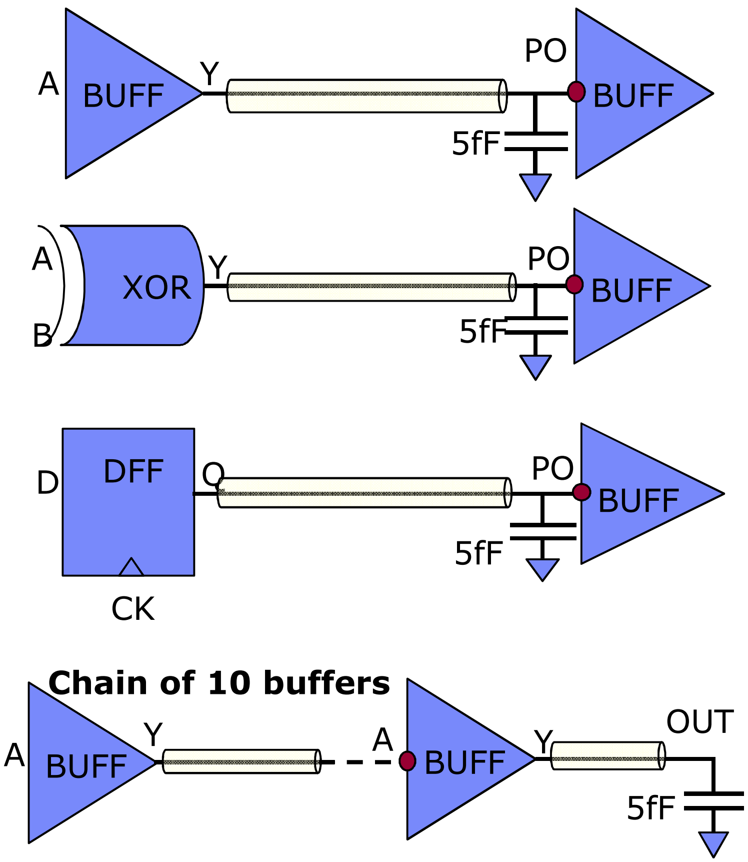
Statistical AT & slew at next gate input

Study of statistical timing models

- **4 methods of statistical timing:**
  - "No CSM" – NLDM instead of CSM
  - "Full CSM" - waveforms for all base corners
    - Base corners waveform are needed for incremental timing
  - "Partial CSM" –nominal waveform with statistical shift&scale
    - Waveforms at other corners are constructed by matching delays and slews of conventional statistical timing
  - "Ramp CSM" – no waveforms stored
    - Gate is modeled with CSM to get delay & slew
    - Linear ramp is propagated through interconnect

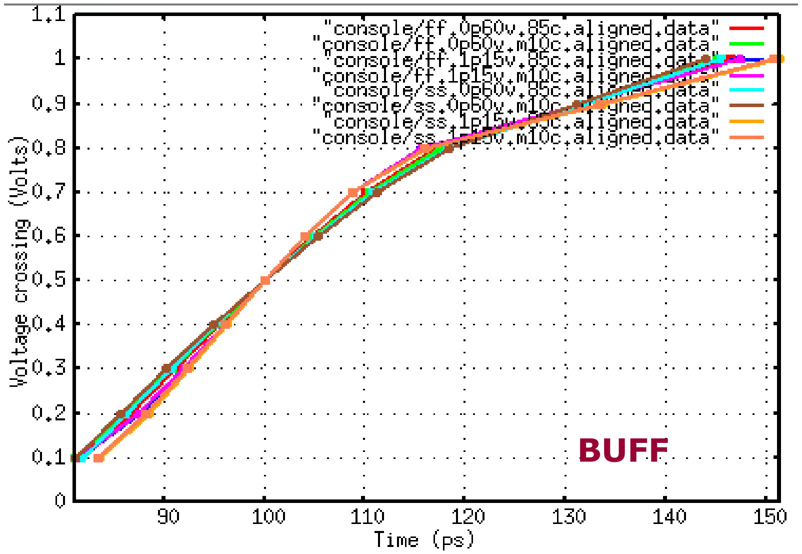
- **8 PVT corners;**
  - FF Vdd = 1.1/0.6 T= 85C
  - FF Vdd = 1.1/0.6 T= -10C
  - SS Vdd = 1.1/0.6 T= 85C
  - SS Vdd = 1.1/0.6 T= -10C
    - Required for PT cross-term

Four 14nm test circuits

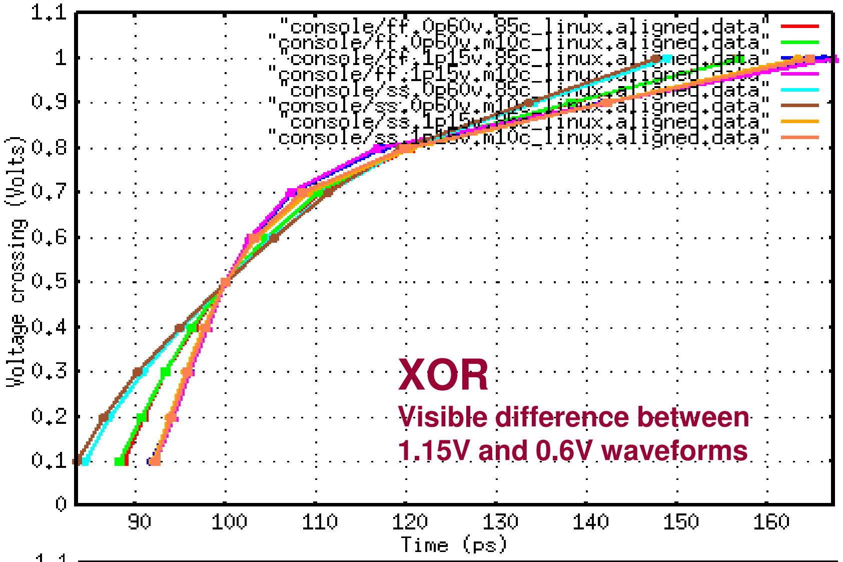


Resistive wire: ***~30-100 fF Ctotal, ~20-40 fF Ceff, 0.3-1 kOhm resistance]***

Aligned corner waveforms

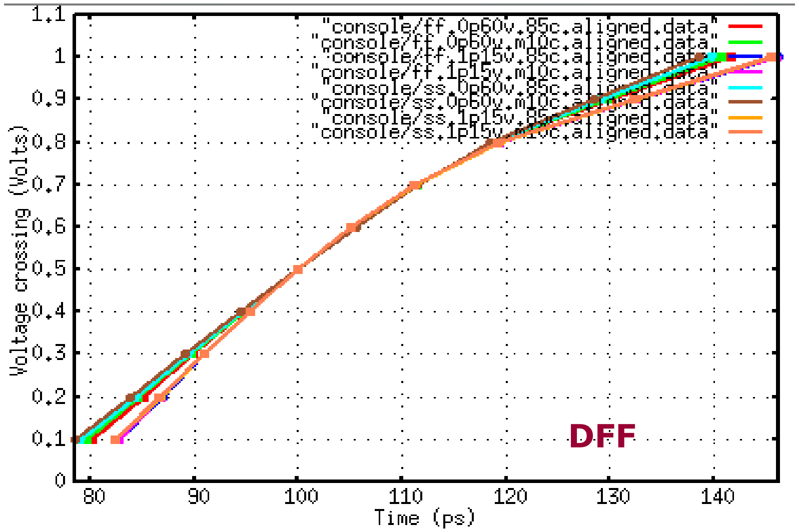


BUFF

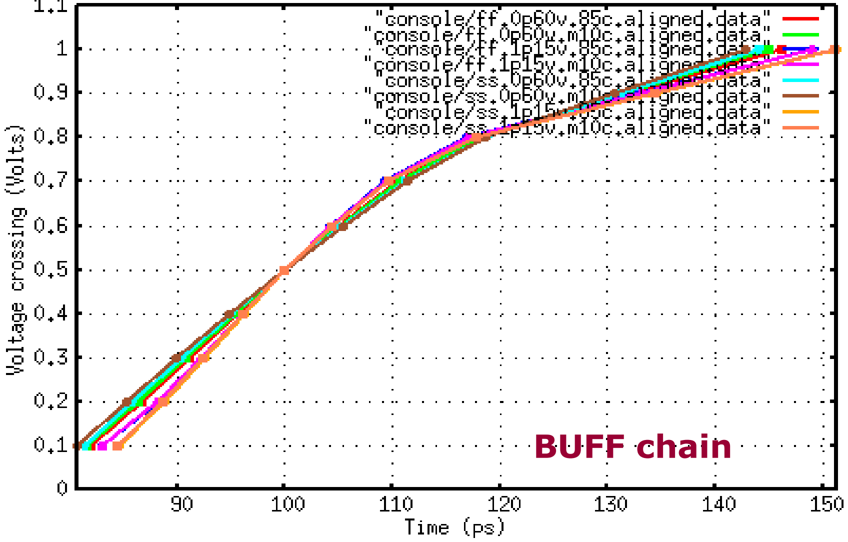


XOR

Visible difference between 1.15V and 0.6V waveforms



DFF



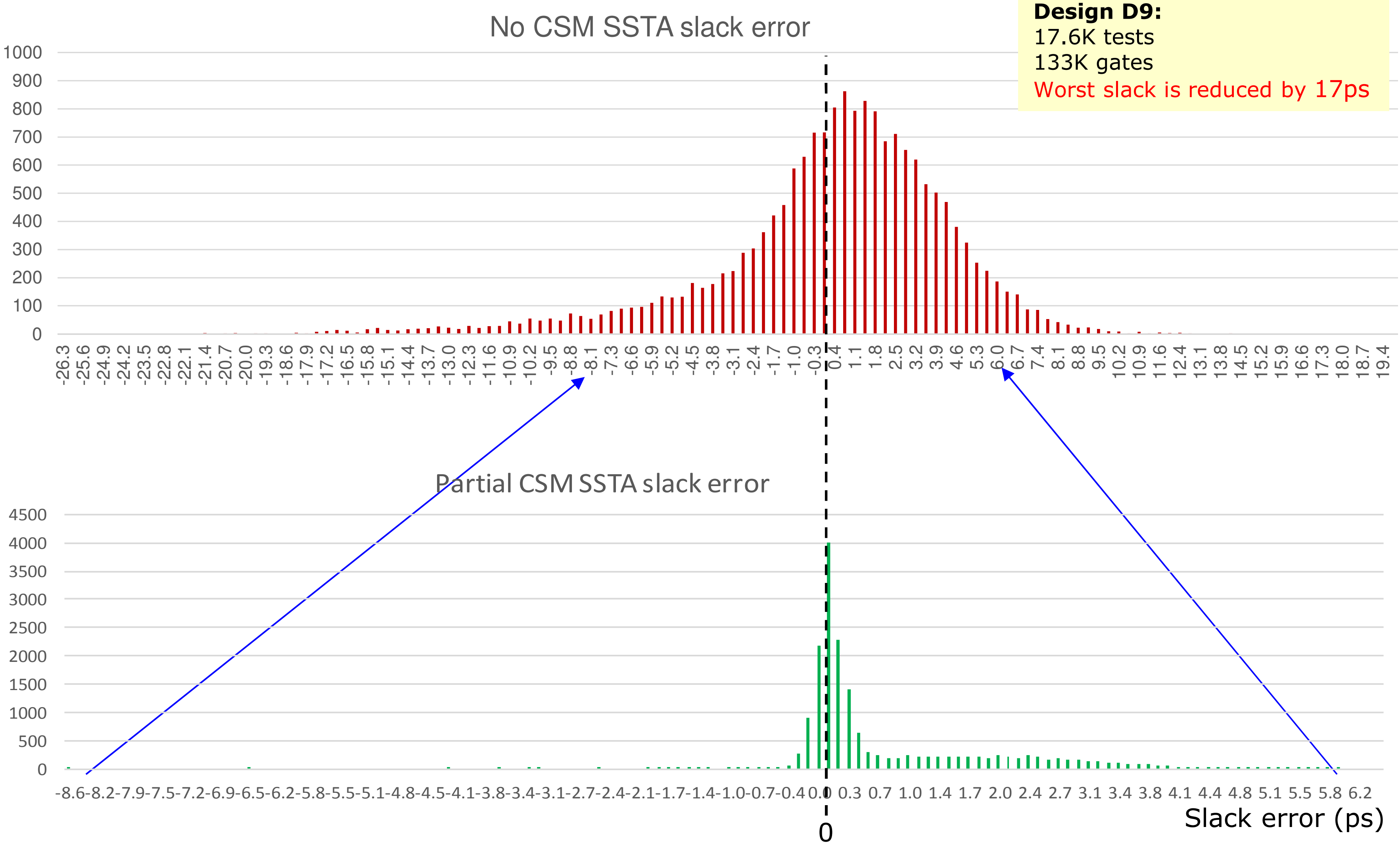
BUFF chain

Base corner selection

Corner P/V/T	Max error of delay/slew (%)				Average error of delay/slew (%)			
	BUFF	XOR	DFF	Chain	BUFF	XOR	DFF	Chain
FF/1.1/-10	4.1/0.6	4.7/4.1	8.1/2.9	2.0/0.27	-1.9/-0.2	-1.4/2.1	1.7/1.5	-0.85/-0.06
FF/1.1/+85	4.4/0.7	3.8/3.8	9.0/2.6	2.0/0.26	-2.1/-0.2	-0.5/1.7	2.3/1.0	-0.84/-0.06
SS/1.1/-10	2.3/0.5	7.5/3.5	12.6/2.6	1.0/0.16	-0.2/0	2.4/1.2	4.7/0.8	-0.04/-0.03
SS/1.1/+85	2.1/0.5	9.1/3.2	13.2/2.4	1.0/0.15	0/0	3.6/0.8	5.0/0.6	-0.04/-0.02
FF/0.6/+85	1.3/0.4	7.7/1.9	7.0/1.7	0.9/0.15	-0.2/0.1	2.1/-0.2	-0.3/-0.3	-0.01/-0.03
FF/0.6/-10	1.0/0.6	6.2/2.0	6.7/1.6	0.9/0.18	-0.2/0.2	0.9/-0.1	-0.6/-0.4	-0.01/-0.04
SS/0.6/+85	1.3/0.8	6.3/1.9	9.9/3.0	1.5/0.05	0.65/0.5	-3.0/-1.2	-5.6/-1.7	0.72/0.02
SS/0.6/-10	0.8/0.9	7.5/1.9	10.7/3.2	1.4/0.05	0.13/0.5	-4.3/-1.3	-6.5/-2.0	-0.59/0

- **Accuracy highly depends on selection of base (nominal) corner**
  - No corner with best accuracy for all circuits both for delays and slews
- **Selected corner with best tradeoff accuracy**

Hold slack error histogram



Design D9:
17.6K tests
133K gates
Worst slack is reduced by 17ps

Timing accuracy, run time, memory footprint

Des-ign	Num gates	Num tests	No CSM AT/Slew Error (%)	CSM AT/Slew Error (%)	Slack Accur Improvment vs No CSM	Run time vs No CSM	Memory vs no CSM
D6	17K	2.1K	1.3/12.1	0.2/0.0	6.9%	16%	3.6%
D7	23K	3.5K	0.1/1.9	0.0/0.2	4.2%	16%	4.6%
D8	30K	6.6K	2.3/13.2	0.5/0.0	5.4%	4%	4.1%
D9	133K	17.6K	1.6/13.2	0.3/0.0	7.1%	15%	15%
D10	170K	34.1K	1.9/13.3	0.3/0.0	1.4%	15%	12.5%
D11	1.63M	196K	1.6/12	0.3/0.1	5.2%	16%	17.5%

- **Typical “No CSM” error in AT 1.3-1.9% (worst 18ps) , in Slew 12-13% (worst 17ps)**
- **Typical “Partial CSM” error in AT 0.3%, in slew 0.0-0.1%**
- **Up to 7% slack improvement (17ps) for representative 250ps clock cycle**
- **Reasonable run time overheads 16%**
- **Additional memory 1-1.5GB per 1M gates**

Conclusions

- **Studied implementations of CSM waveforms in statistical timing for 14nm high performance designs**
  - Naïve approach results in manifold memory overhead
- **Developed method of propagating statistical waveforms**
  - Statistical shift and scale technique was modified for better performance and lower memory footprint.
- **Achieved substantial slack accuracy improvement**
  - Up to 17ps, i.e. 7 of 250ps cycle time
- **Run time increase does not exceed 16%**
- **Memory overhead is about 1.1GB per 1M gates**
  - Does not exceed 17.5%
- **Further accuracy improvement can be achieved**
  - Dynamic selection/construction of nominal corner for shift and scale representation