Highly-dense Mixed Grained Reconfigurable Architecture with Via-switch

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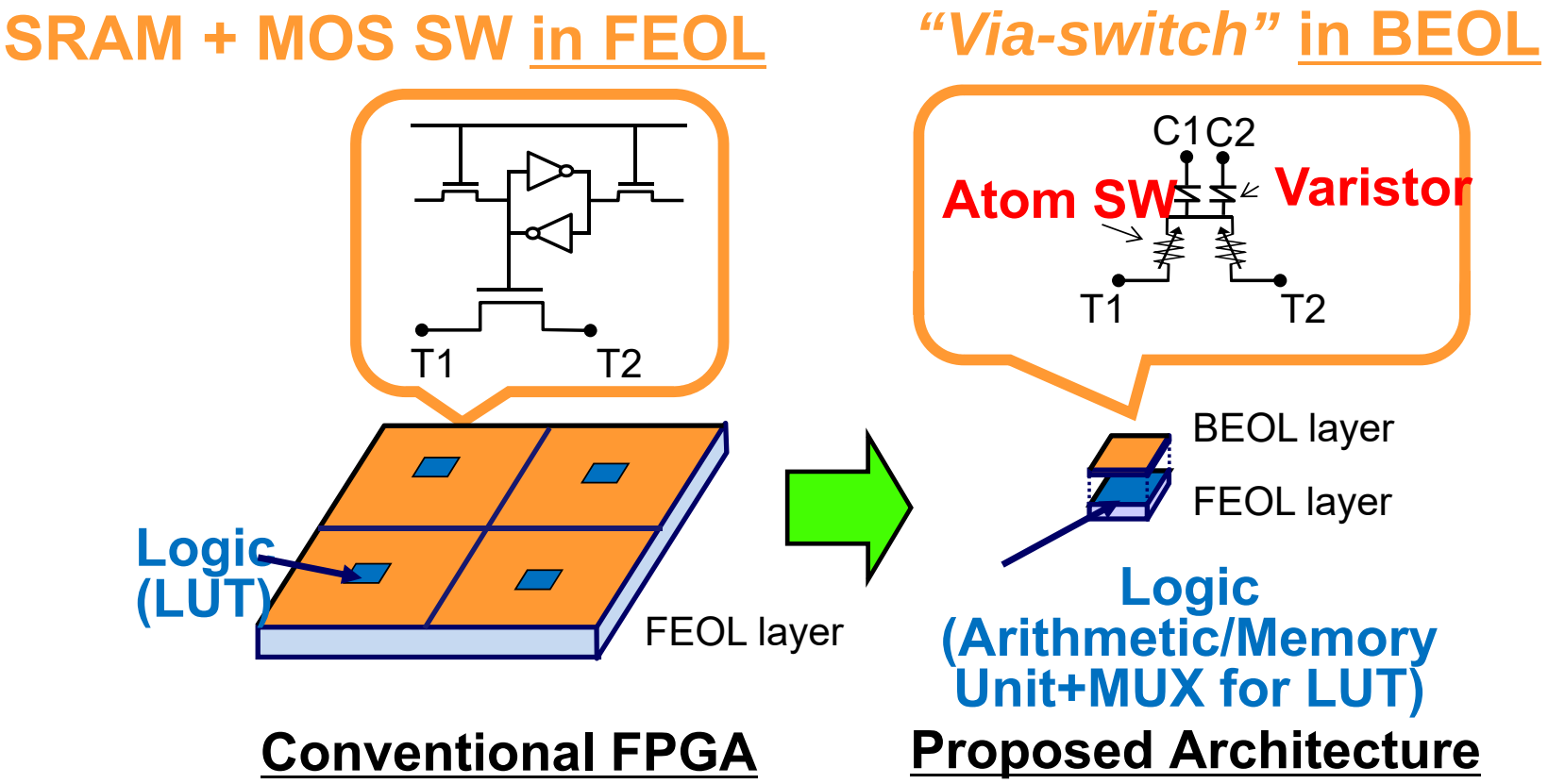
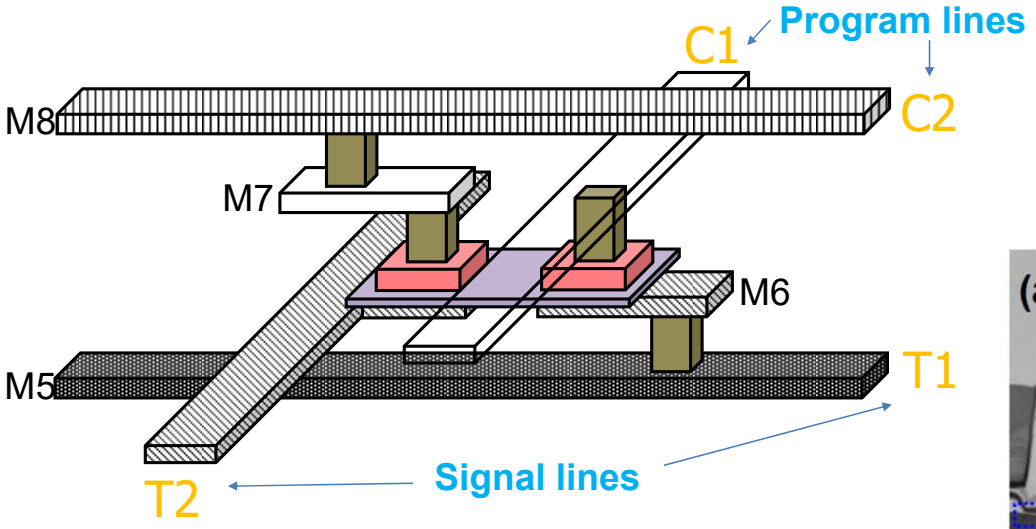
Contribution

26X higher density
66% smaller interconnect delay at 0.5V

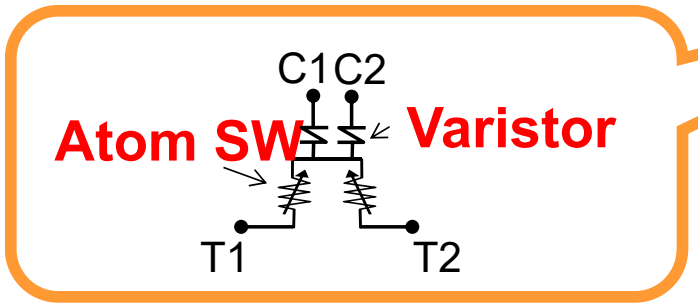


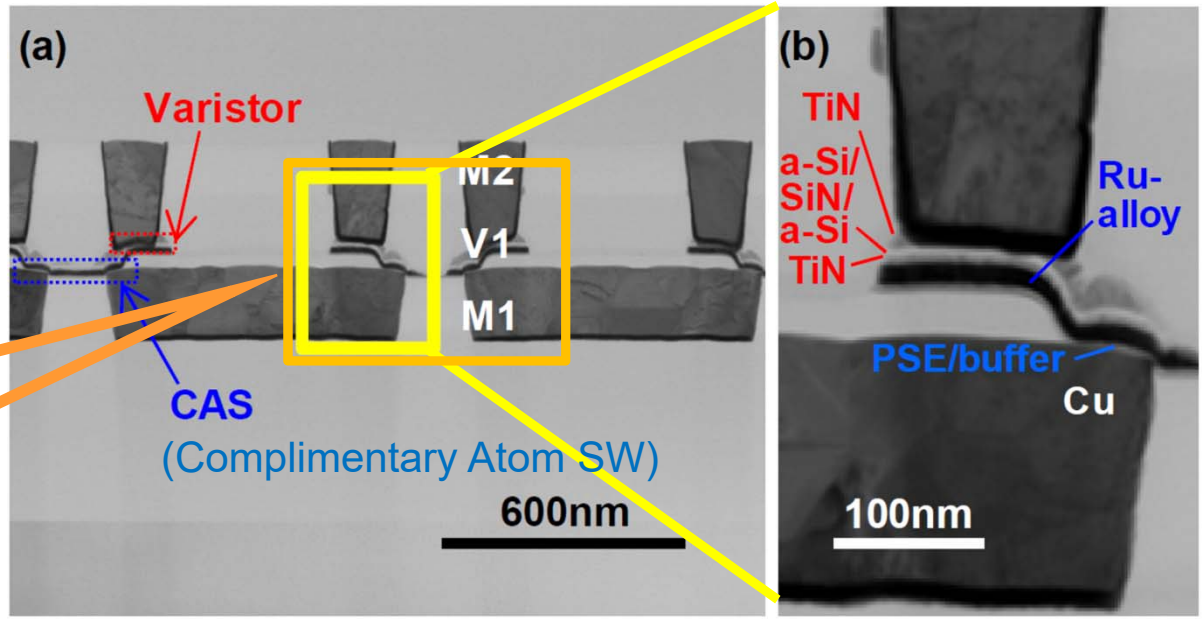
Via-switch



Access Tr. unnecessary for programming

[Banno, IEDM2015]

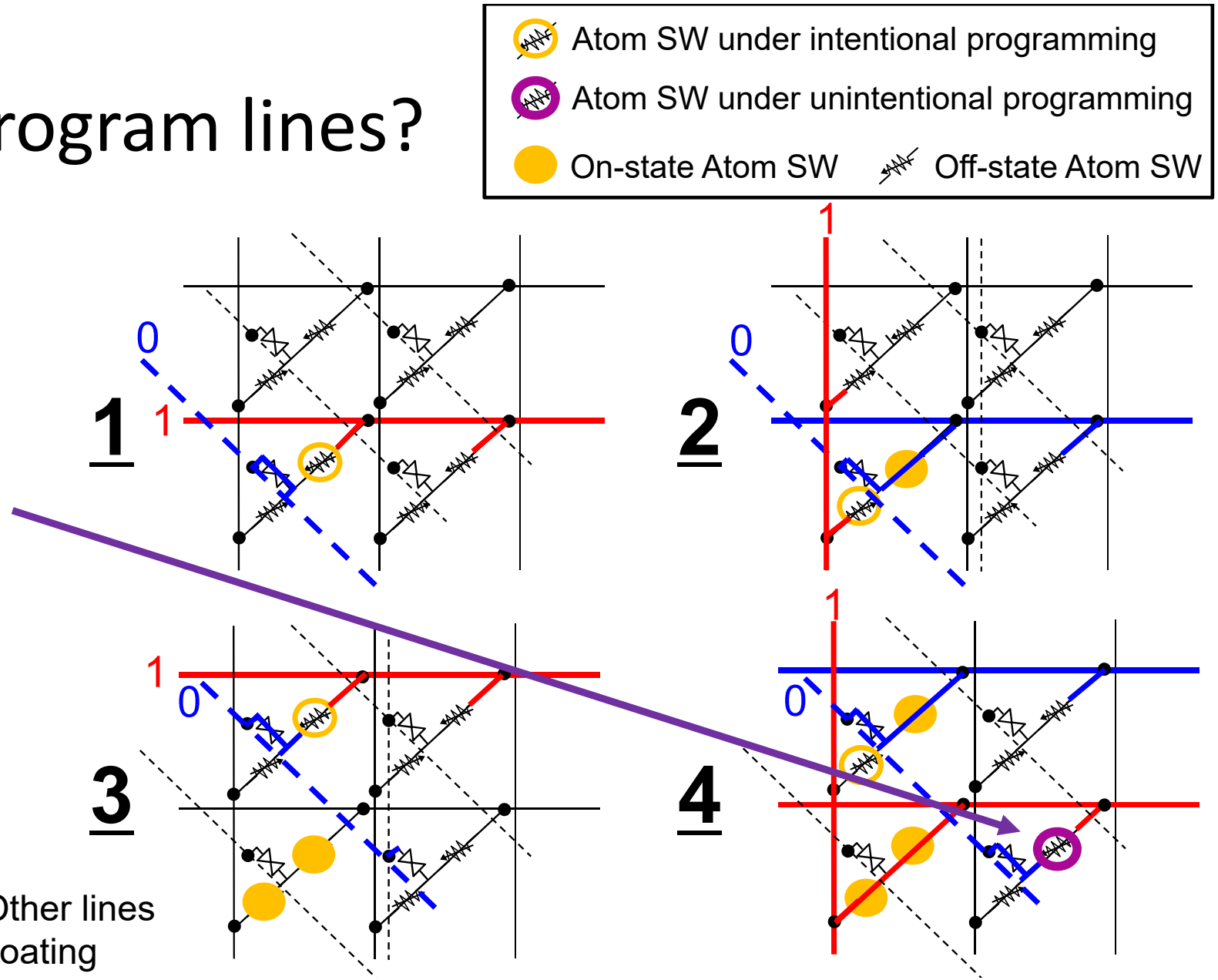




Atom SW: Electrochemical nonvolatile R-change device
On-R can be reduced to 200Ω.

Why two program lines?

With a single program line, unintentional programming will happen.

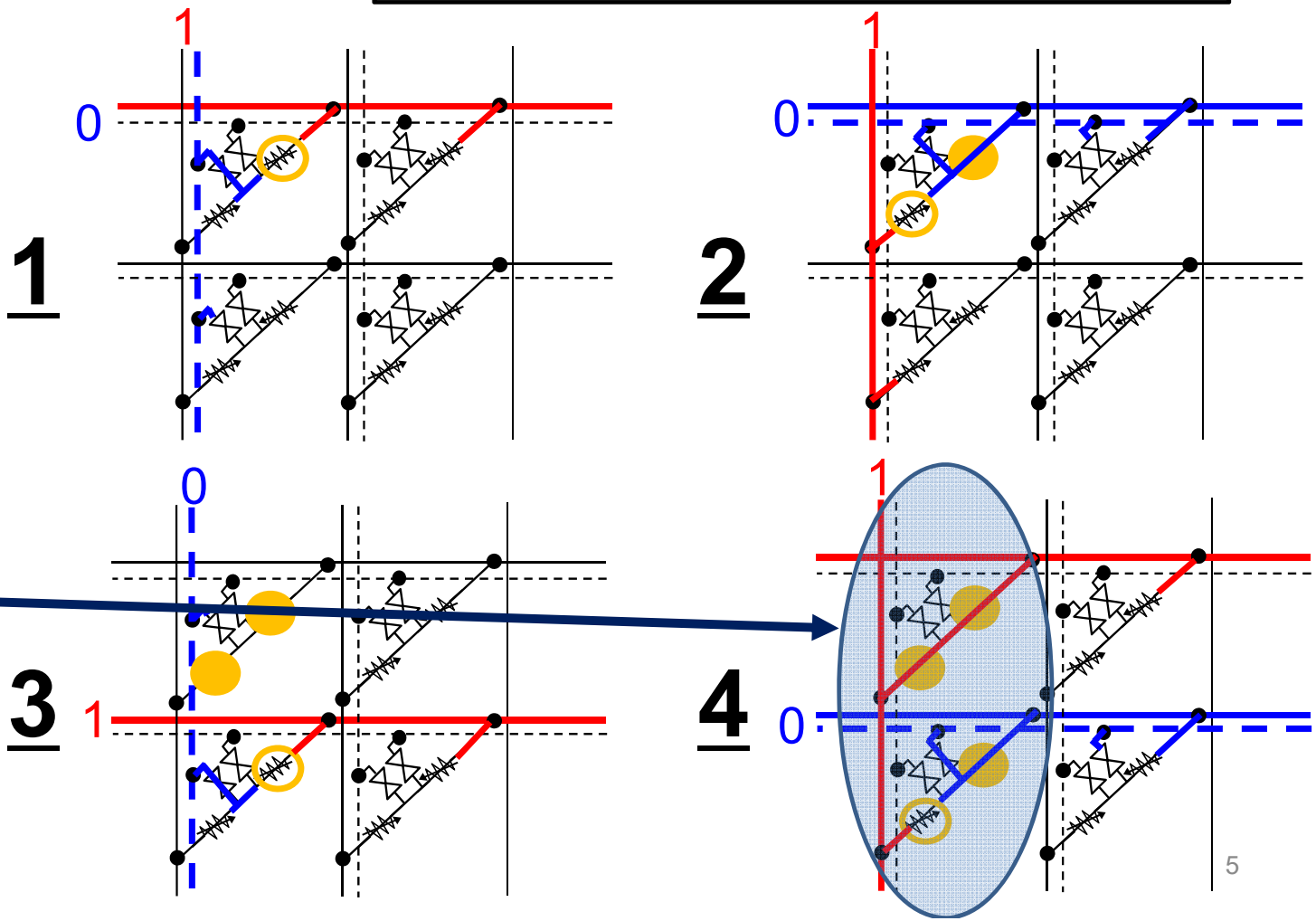


Why two program lines?

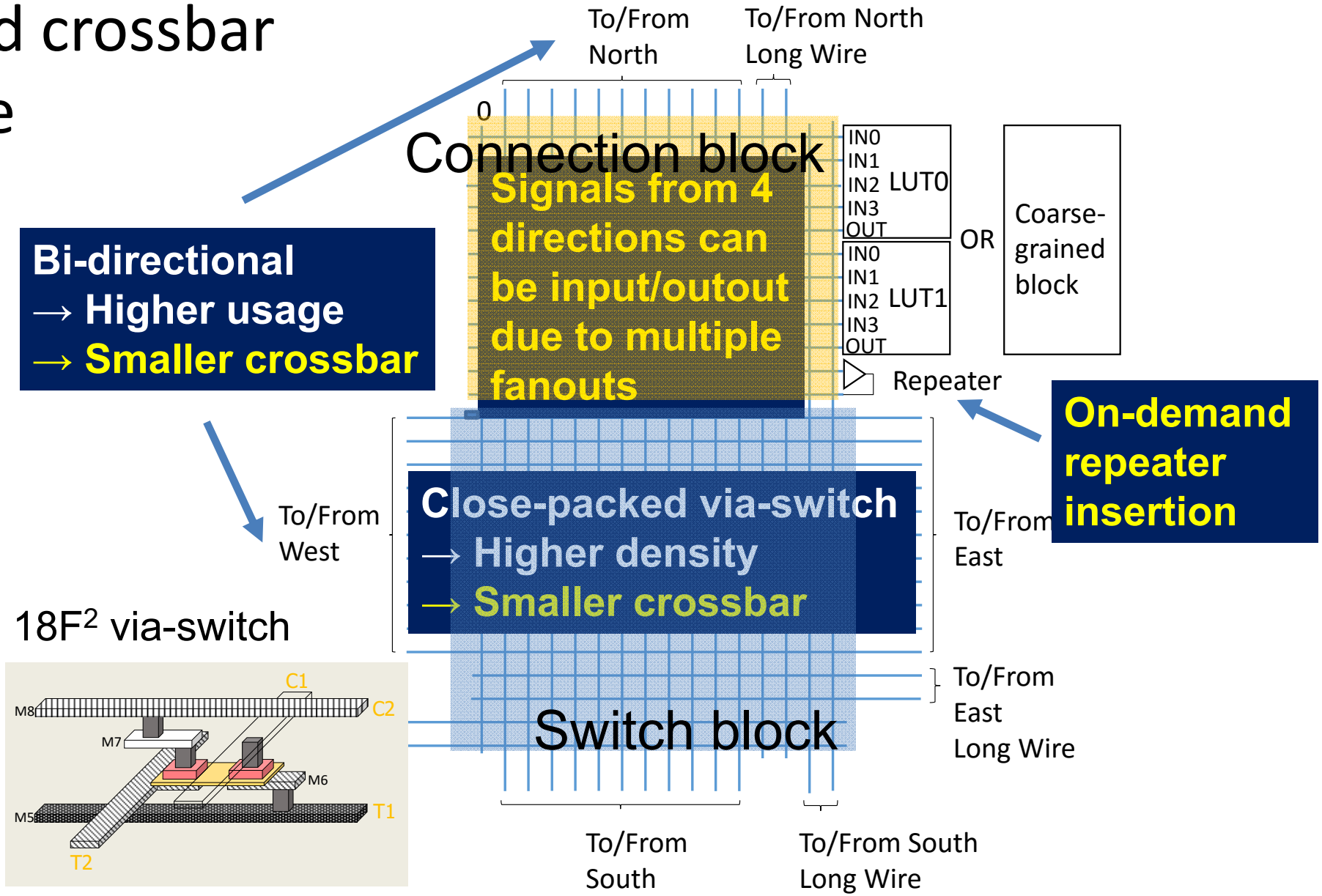
With two program lines, unintentional programming will not happen.

Multiple-ON in a column enables multiple fanouts.

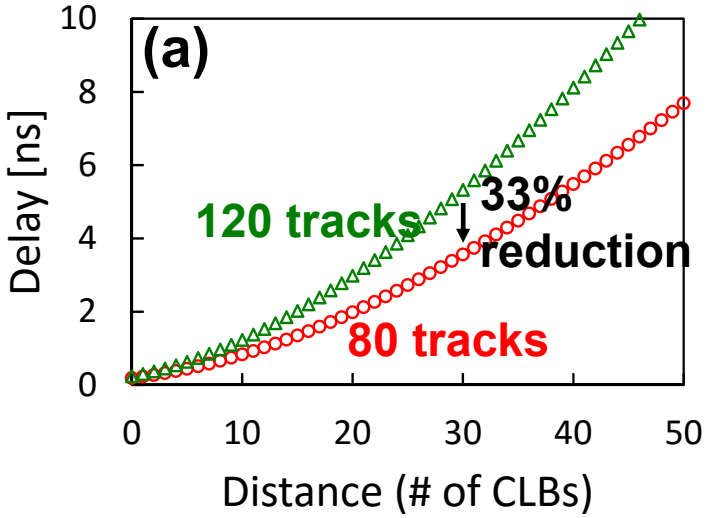
Other lines floating

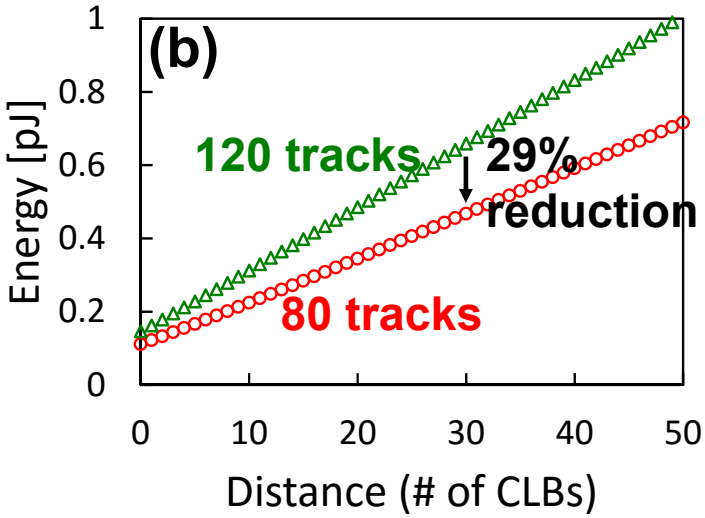


Proposed crossbar structure



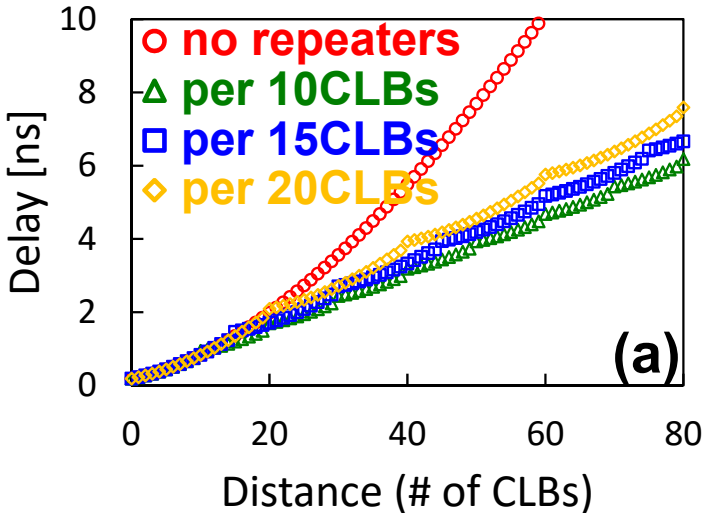
Interconnect Performance Evaluation (65nm)

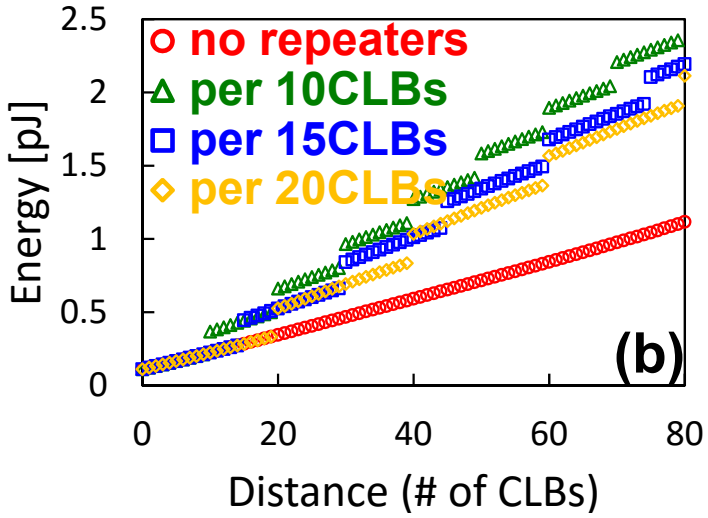




Smaller crossbar thanks to bidirectional signaling reduces delay and energy.

117x80 or 157x120 crossbars
No repeaters
@1.0V





Delay/energy can be optimized by flexible buffering.

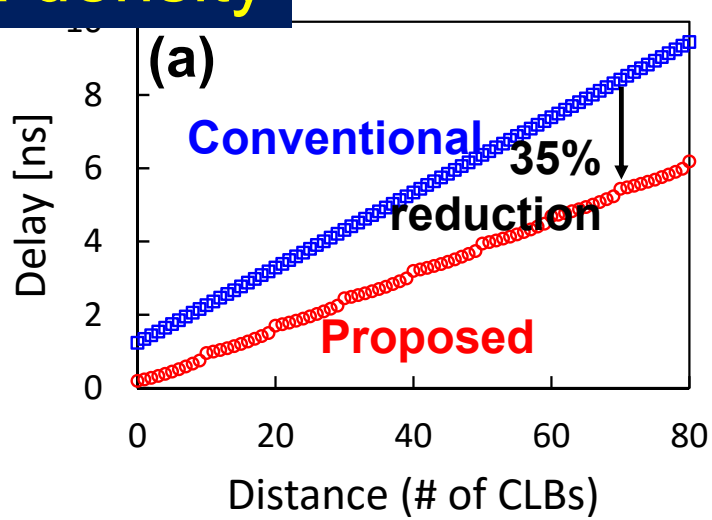
117x80 crossbar
@1.0V

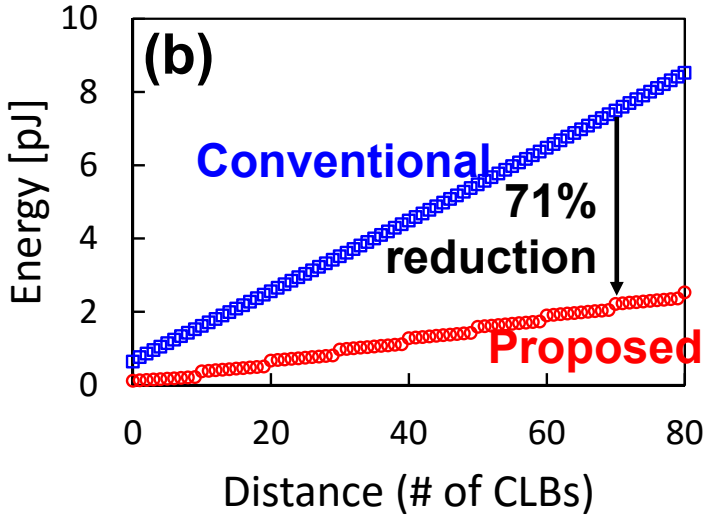
Comparison w/ SRAM-based FPGA (TMG+SRAM crossbar)

26X higher area density

1.0V

117x80 crossbar
repeater inserted

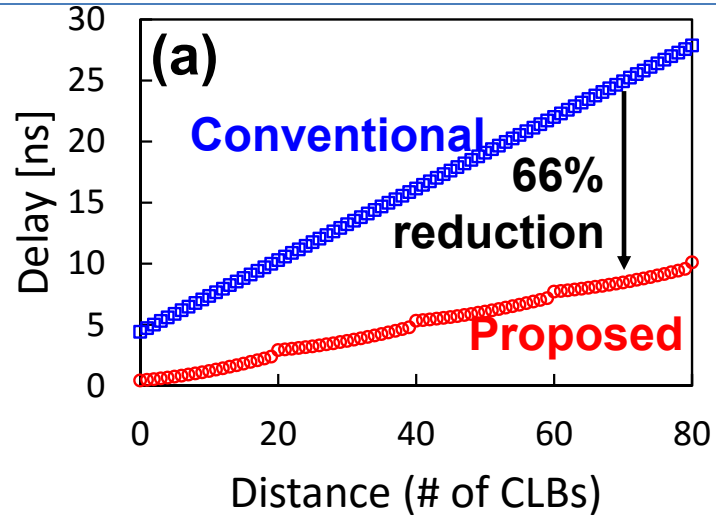


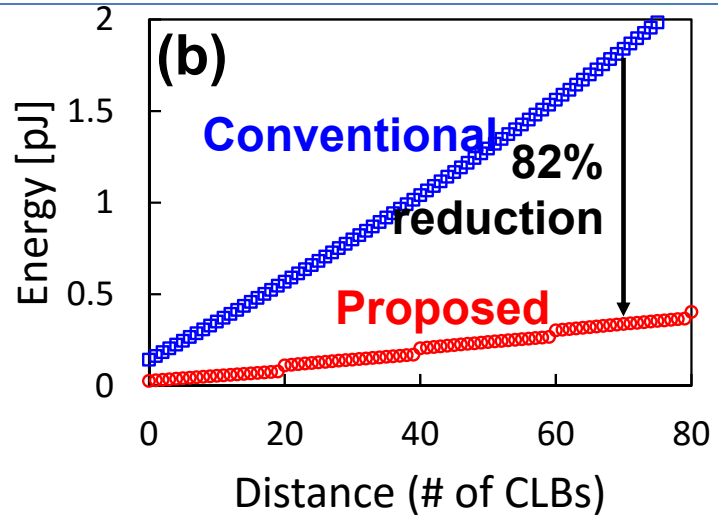


0.5V

On-R of via-switch is independent of supply voltage.

117x80 crossbar
repeater inserted





Conclusion

- Proposed a highly-dense reconfigurable architecture that exploits via-switch.
  - 26X higher density
  - Interconnection delay is reduced by 35% (1.0V) and 66% (0.5V)
  - Interconnection energy is reduced by 71% (1.0V) and 82% (0.5V)
- Future works
  - Import long wire interconnection
  - Application mapping and performance evaluation