Relative Placement in Timed Asynchronous Design

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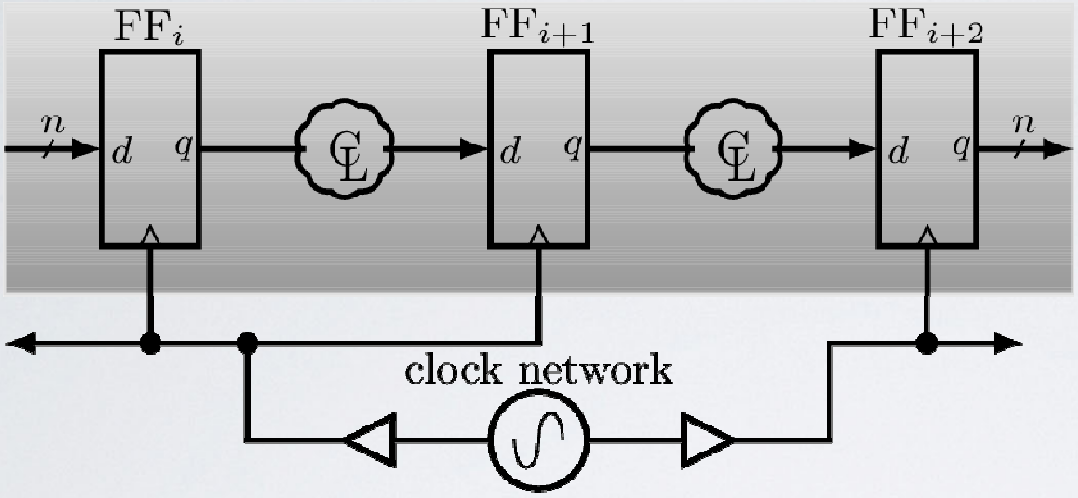
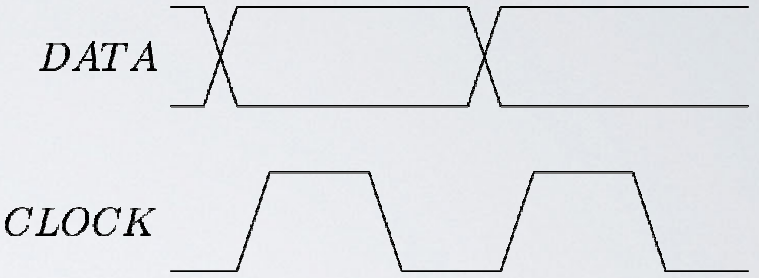
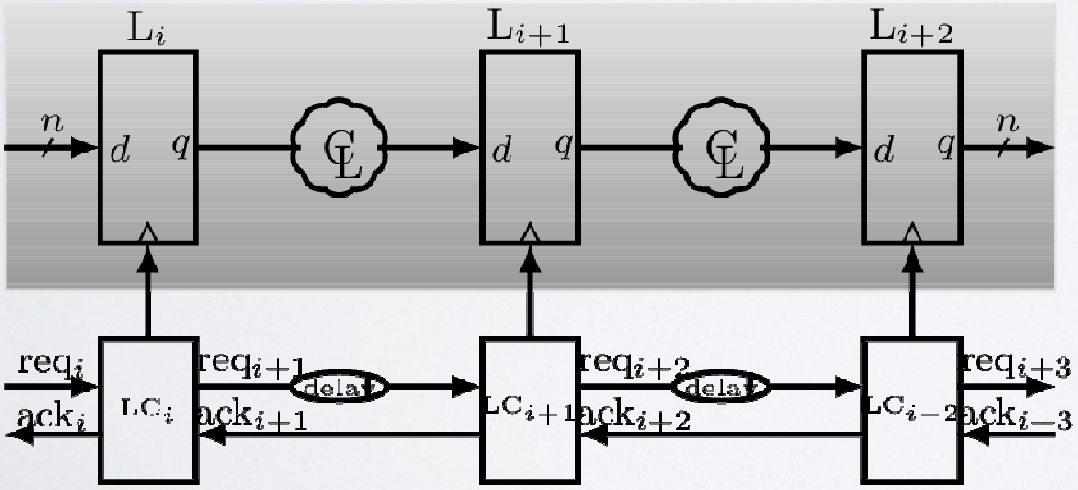
Overview

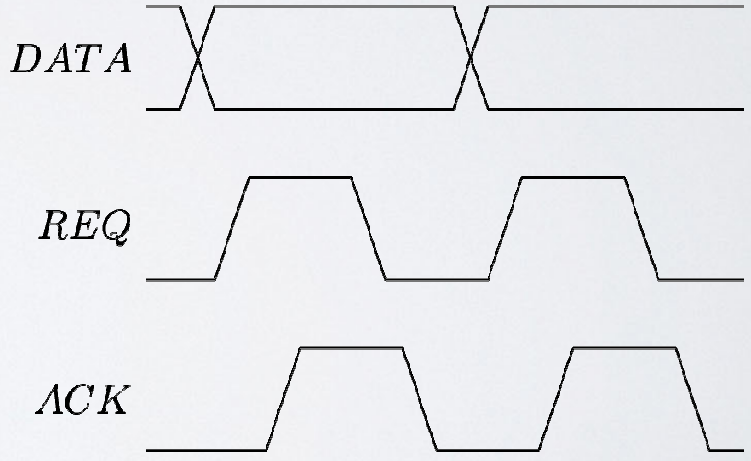
- Background
- Relative Placement
- Results
  - Multiplier & Encryption ASIC

ASYNCHRONOUS 4-PHASE HANDSHAKE

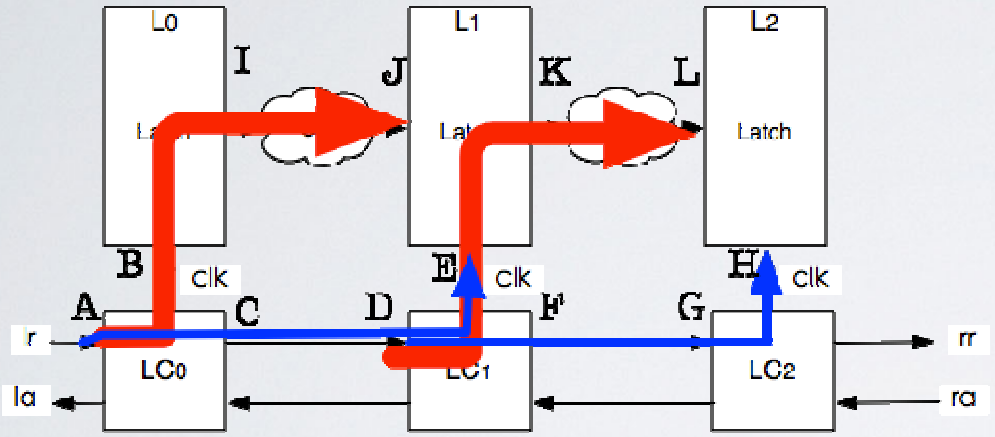


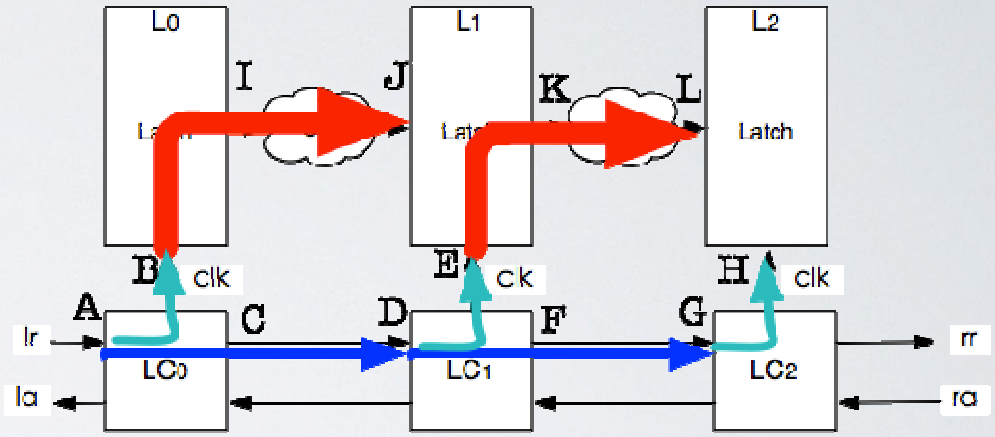






RELATIVE TIMING

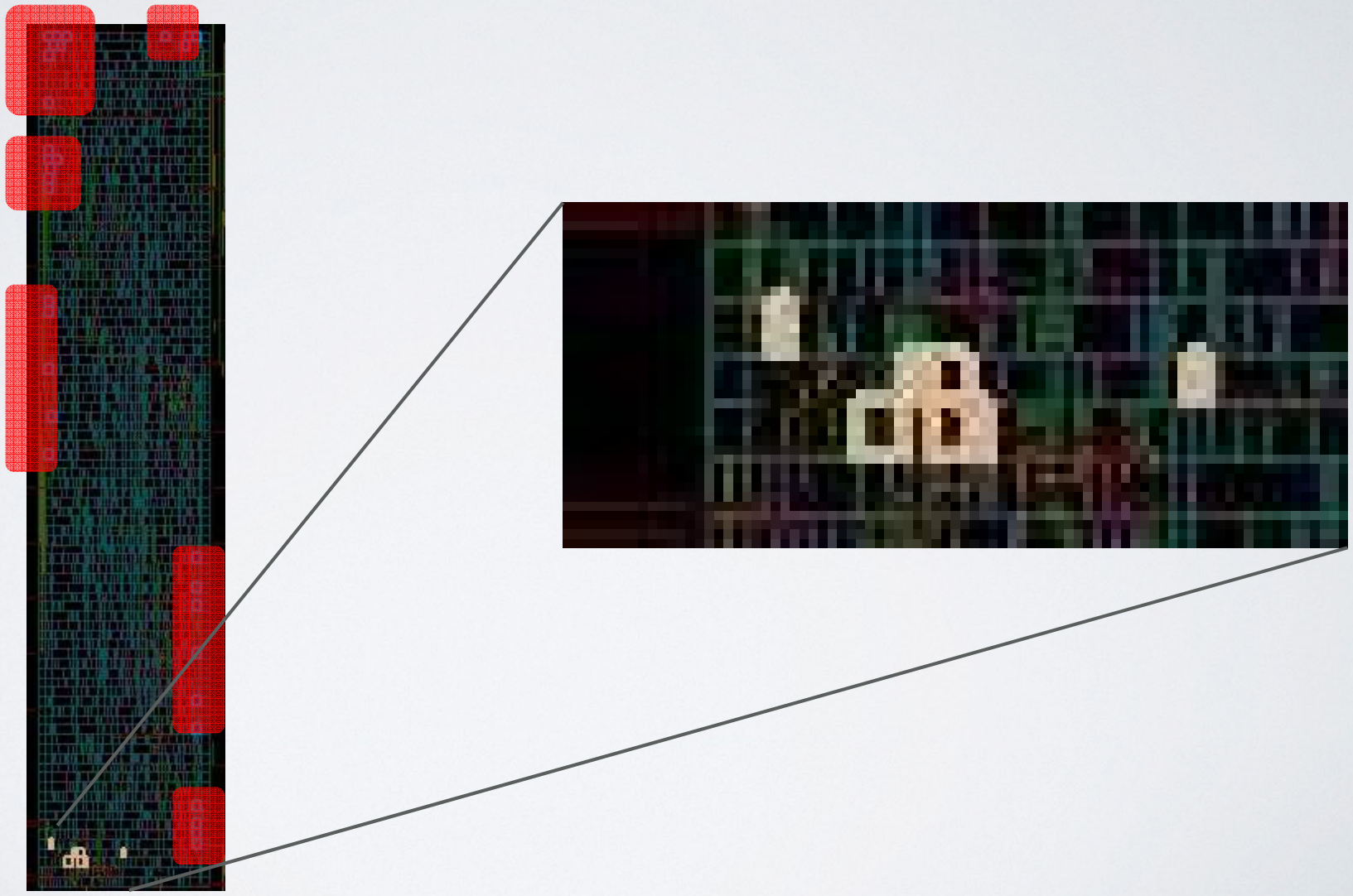




$$LC_0/lr \mapsto L_1/d{+}m \prec LC_1/clk$$
$$LC_1/lr \mapsto L_2/d{+}m \prec LC_2/clk$$

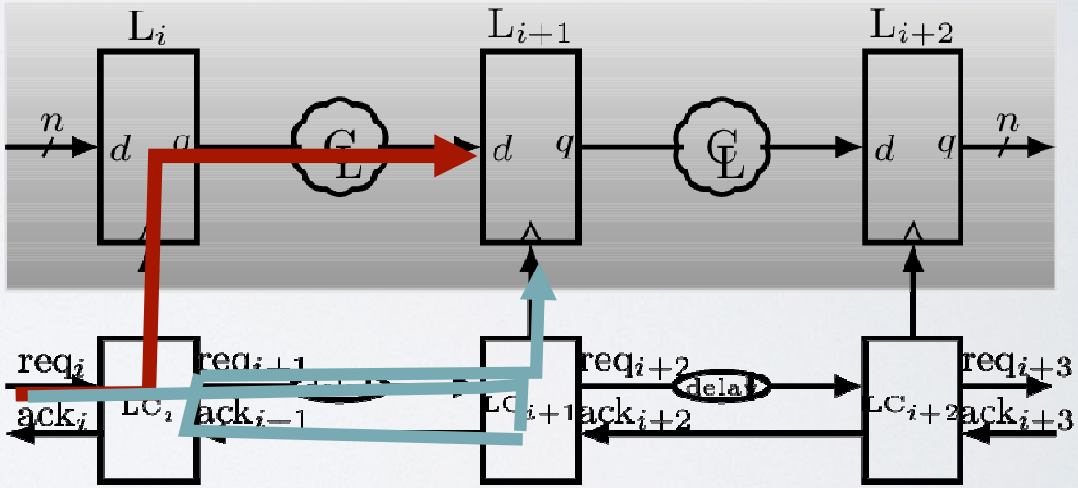
set_max_delay $dpdelay -from L_0/clk -to L_1/D	(1)
set_min_delay $cdelay_min -from LC_0/lr -to LC_1/lr	(2)
set_max_delay $ckdelay -from LC_0/lr -to L_0/clk	(3)
set_max_delay $dpdelay -from L_1/clk -to L_2/D	(4)
set_min_delay $cdelay_min -from LC_1/lr -to LC_2/lr	(5)
set_max_delay $ckdelay -from LC_1/lr -to L_1/clk	(6)
set_max_delay $ckdelay -from LC_2/lr -to L_2/clk	(7)

TIMING DRIVEN PLACEMENT



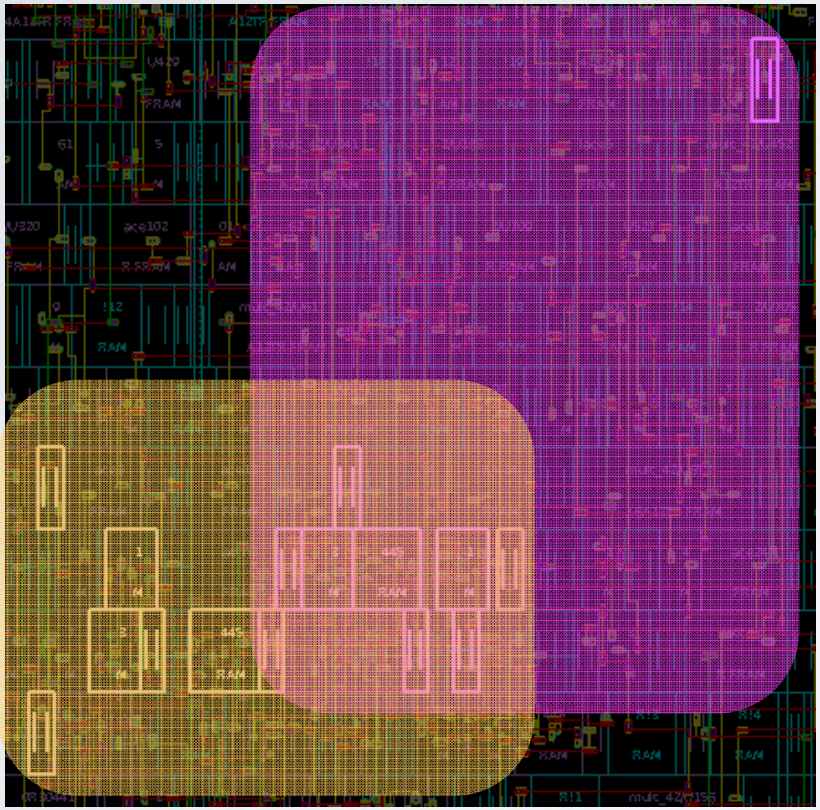
FULL PATH TIMING VALIDATION

- Slack Calculation
  - Delay difference between min-path and max-path

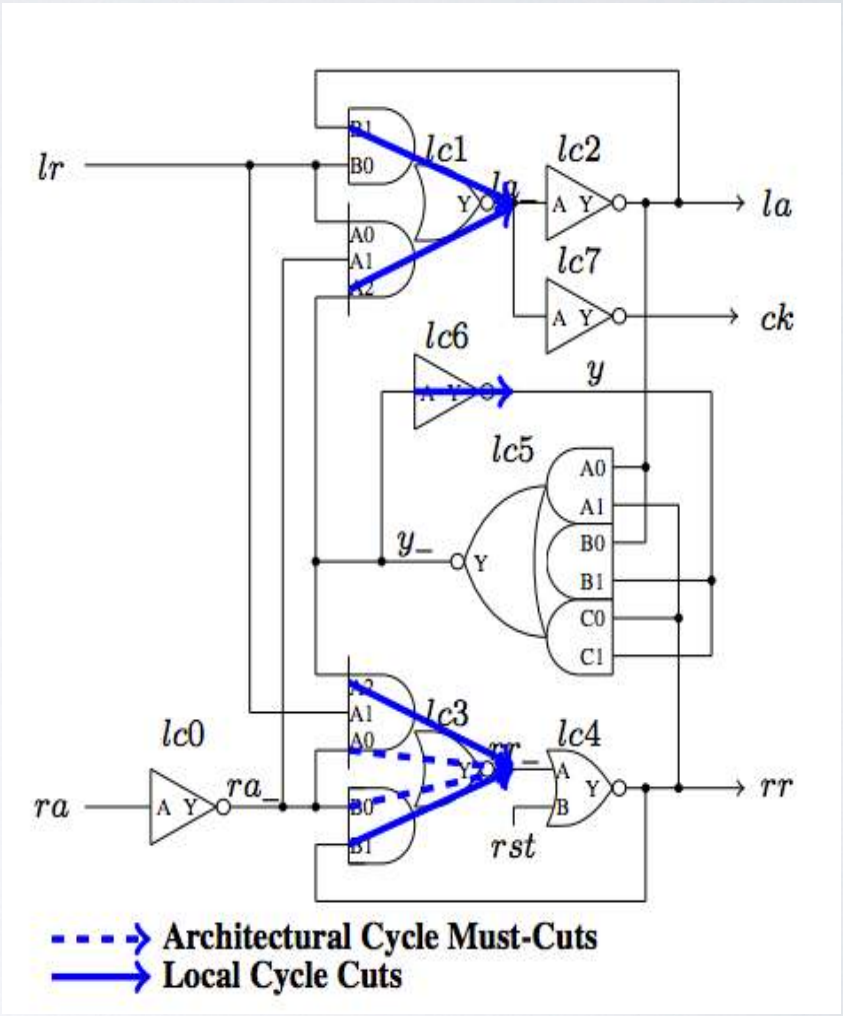


RELATIVE PLACEMENT

Bounding Boxes



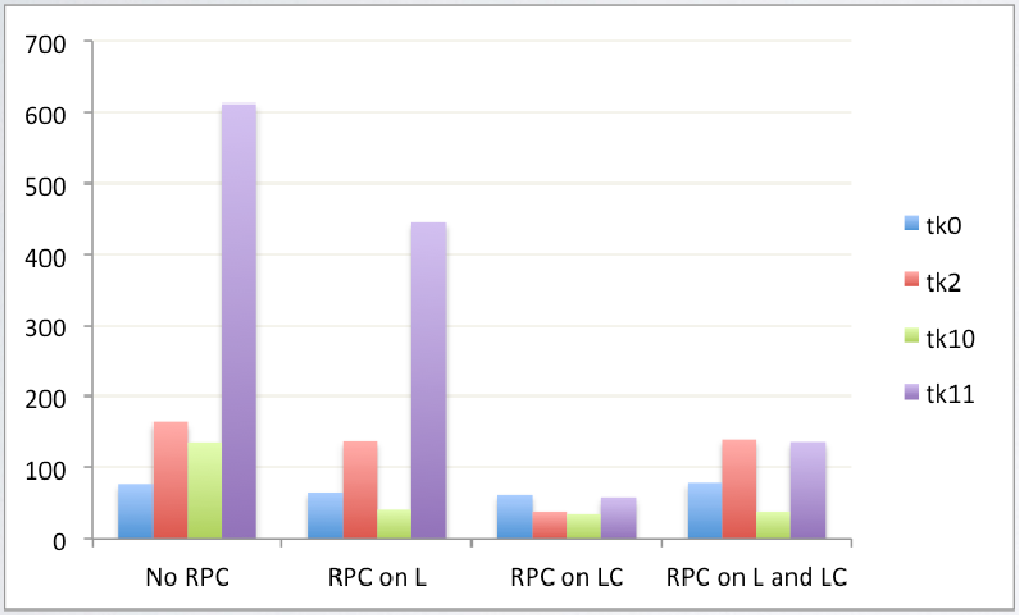
Without Relative Placement

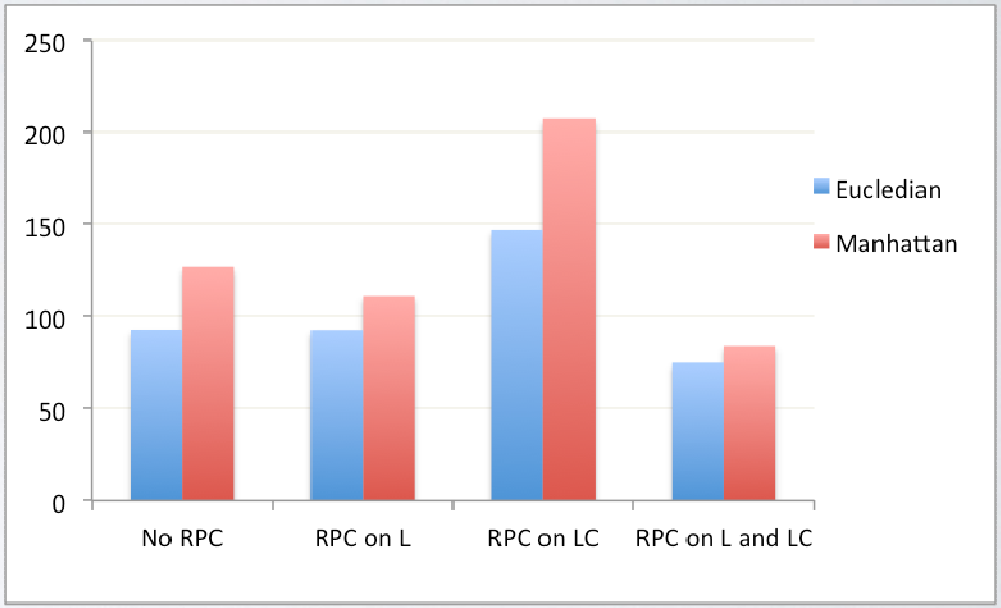


REPORTS

- XY bounding box for hierarchical blocks
- Euclidian / Manhattan Distance between connected blocks
- Chip Area
- Cycle Time
- Slack
- Total Wire Length
- Power

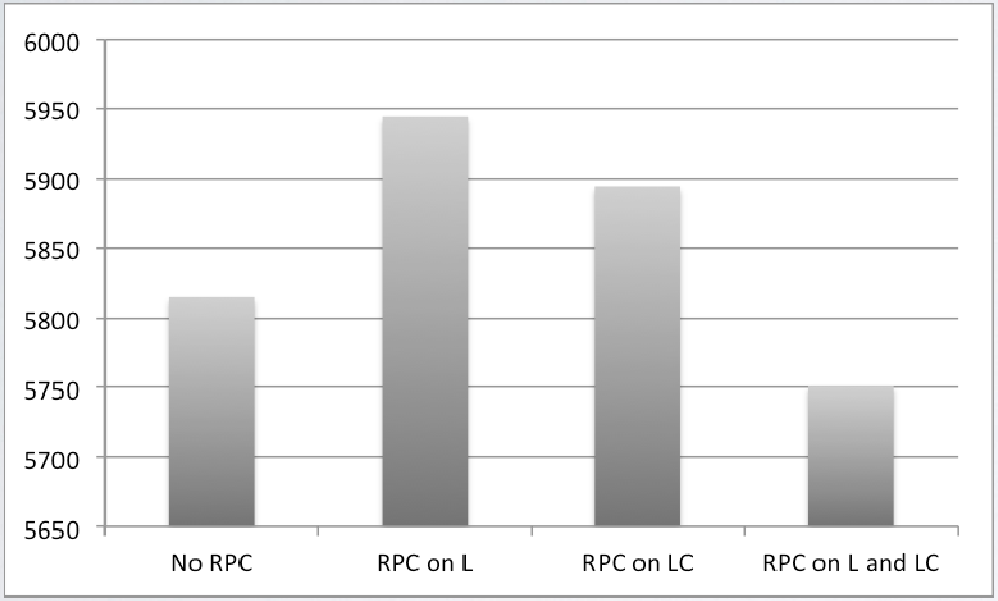
MULTIPLIER



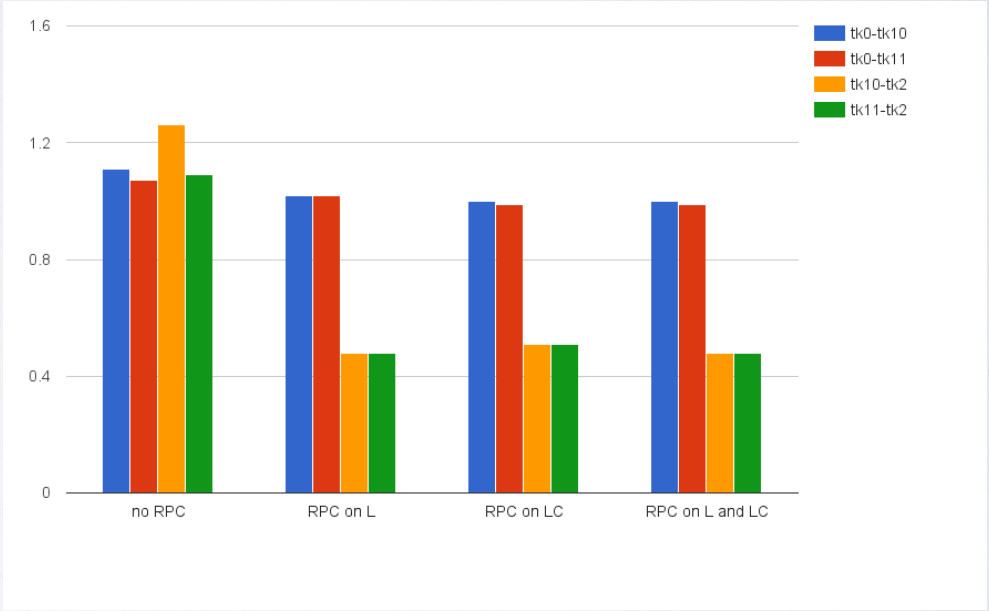


Bounding Area (μm^2) Total Distance Between Blocks (μm

MULTIPLIER

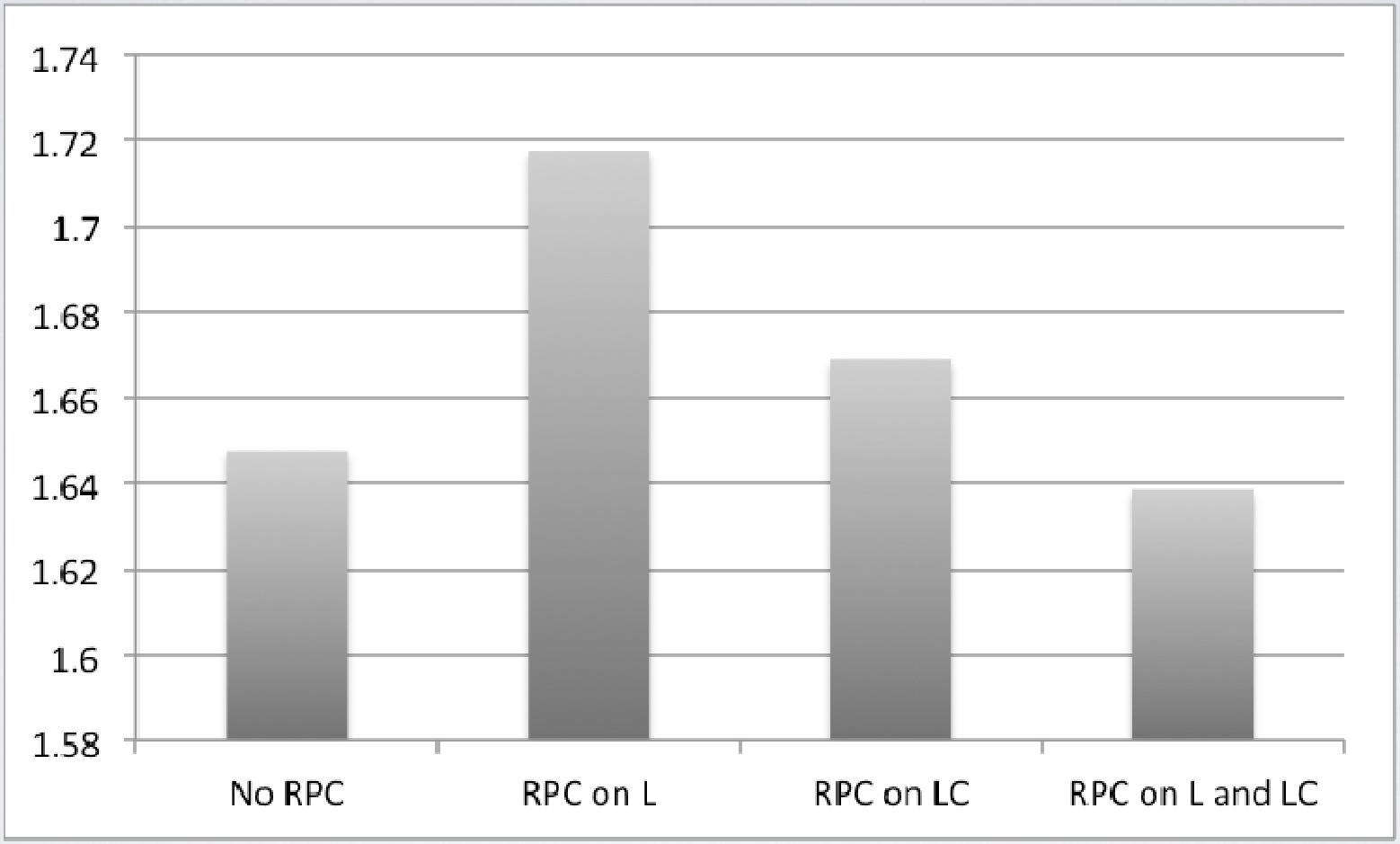


Area (μm^2)



Cycle Time (ns)

MULTIPLIER

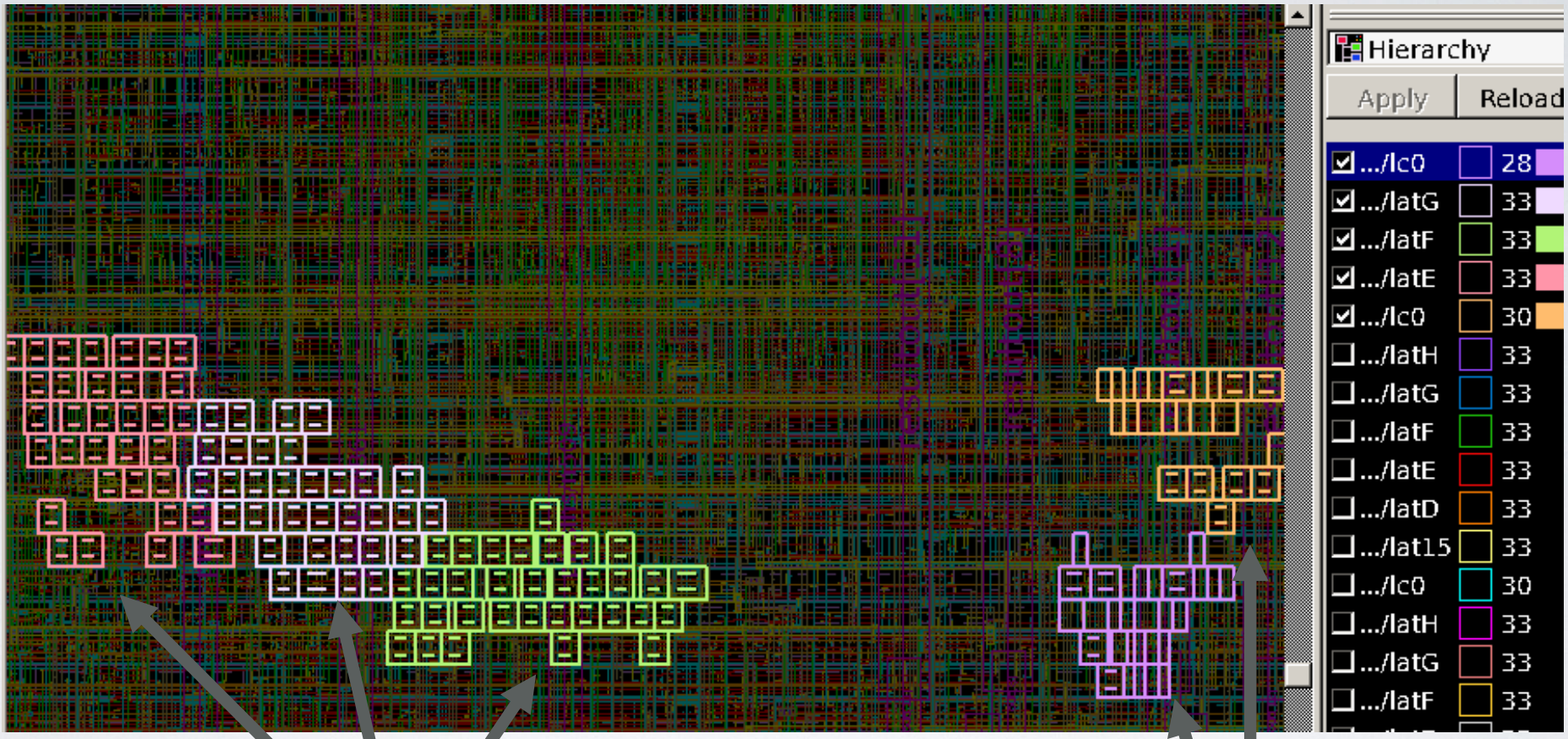


Power (mW)

ENCRYPTION ASIC

- 3 Million transistors
- 2,800 timing constraints
- 4,500 relative placement constraints

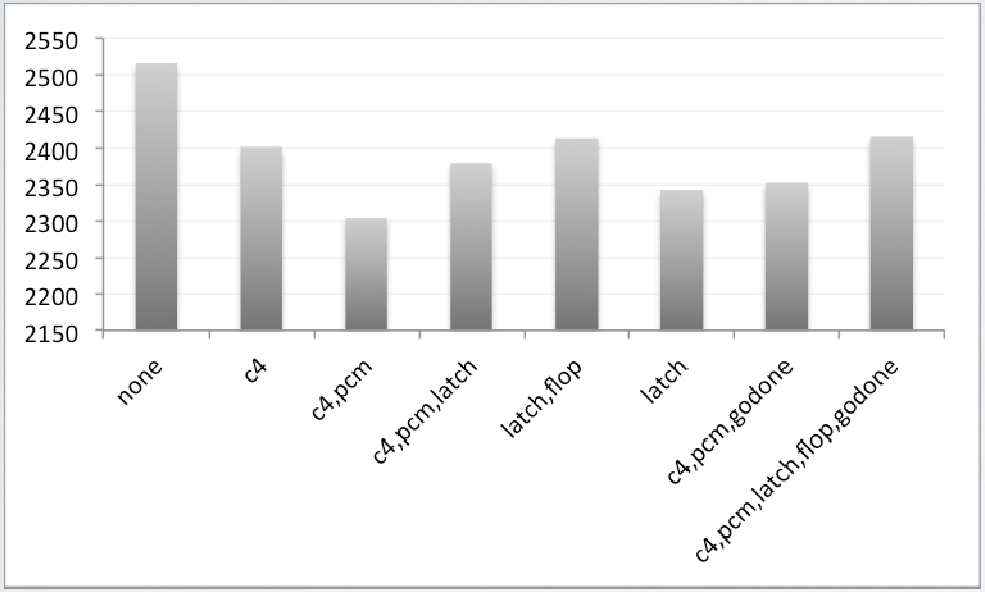
ENCRYPTION ASIC



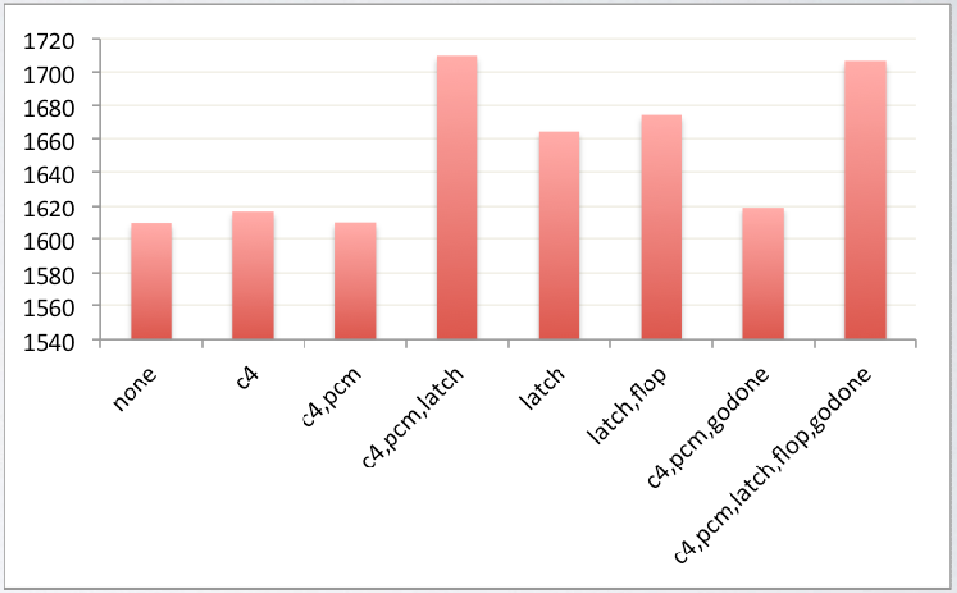
Latch Banks

Linear Controllers

ENCRYPTION ASIC



Cycle Time (ps)



Energy (pj)

Energy Delay Product: 10% improvement

CONCLUSION

- Relative Placement Helps Timing Driven PnR
- Slack Optimization
- Performance Benefits

QUESTIONS?