Accurate Timing Updates for Circuit Optimization without Explicit Parasitic Data

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Outline

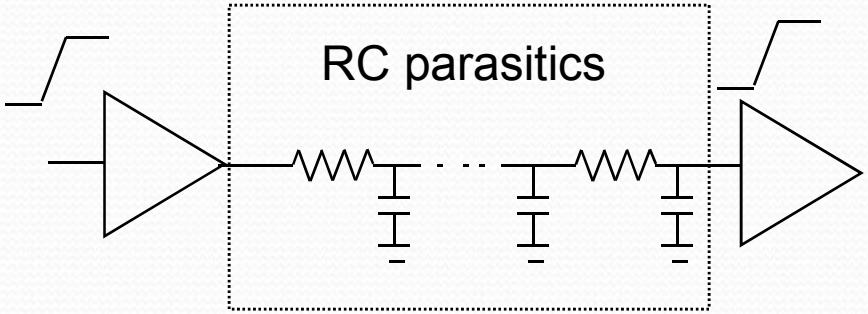
- Motivation
- New approach to update timing in circuit optimization **without explicit parasitic data**.
- Results and Conclusion

Motivation

- Our in-house tool fixing timing violations
  - Need quick timing estimation with good accuracy
  - Timing data from reference timer as a starting point
  - Need light weight without using netlist parasitic

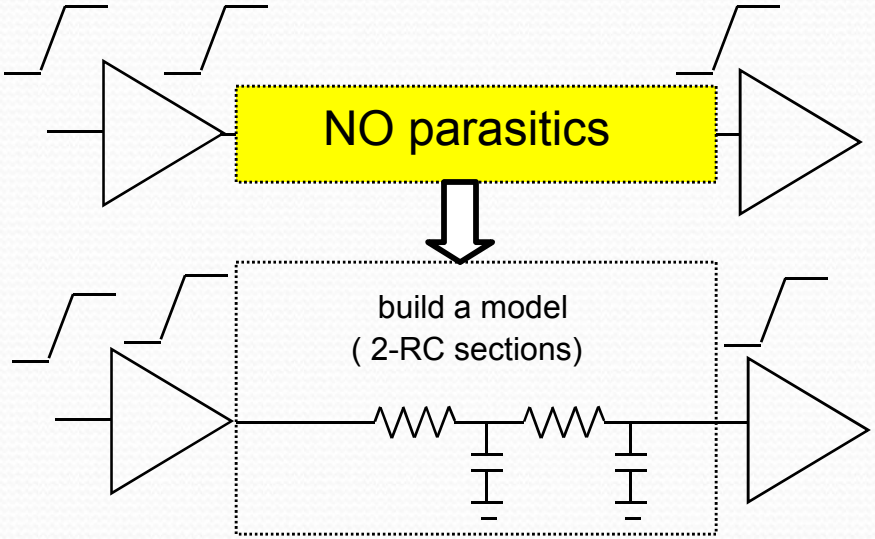
Method to estimate timing without parasitics

- Traditional delay/slew estimation



- Compute delay/slew by:
  SPICE, AWE, RICE, PRIMA, D2M, S2M, etc.

- Our estimation flow



- Compute new delay/slew after gate sizing by: D2M, S2M.
- Memory saved from parasitics. Runtime saved from parasitic reduction

How to construct net model?

- Known data before sizing gates: **tr, d, s, C_{total}, C_L**

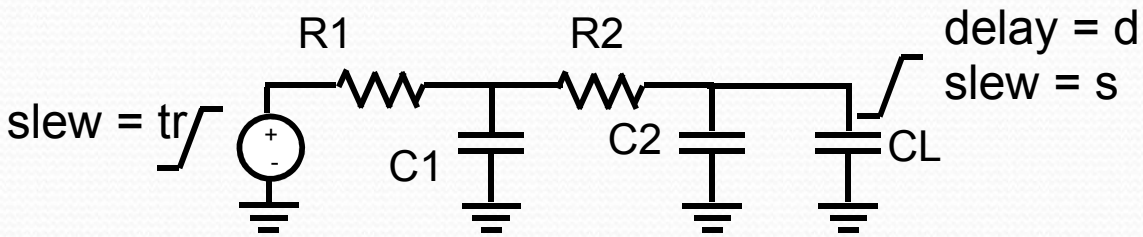


Figure 2: Net model computation

- First, find two moments **m1** and **m2** from **tr, d, s**
- Compute **R1** and **R2** from **m1** and **m2**

Net Model: Leverage D2M and S2M reversely

- D2M (Ref [5])
  - Step input: $Delay_{\_D2M} = \frac{m_1^2}{\sqrt{m_2}} \ln 2$
  - Ramp input: $Delay_{\_D2M_{ramp}} = -(1-\alpha)m_1 + \alpha * Delay_{\_D2M}$ (1)

$$\alpha = \left(\frac{2m_2 - m_1^2}{2m_2 - m_1^2 + tr^2/12} \right)^{\frac{5}{2}}$$

- S2M (Ref [7])
  - Step input: $Slew_{\_D2M} = \frac{\sqrt{-m_1}}{\sqrt[4]{m_2}} \ln 9 \sqrt{2m_2 - m_1^2}$
  - Ramp input: $Slew_{\_D2M_{ramp}} = \sqrt{Slew_{\_D2M}^2 + tr^2}$ (2)

Net Model: Compute moments m1 and m2

- The relationships between **m1**, **m2** and **d**, **s** and **tr** are

$$\begin{cases} -(1-\alpha)m_1 + \alpha * \dfrac{m_1^{\,2}}{\sqrt{m_2}} \ln 2 = d \\ \dfrac{-m_1}{\sqrt{m_2}} (\ln 9)^2 (2m_2 - m_1^{\,2}) + tr^{\,2} = s^2 \end{cases} \qquad (3)$$

- Solving (3) iteratively w. r. t. α (initial $\alpha = 1$)

- For fixed α , (3) reduces to cubic equation

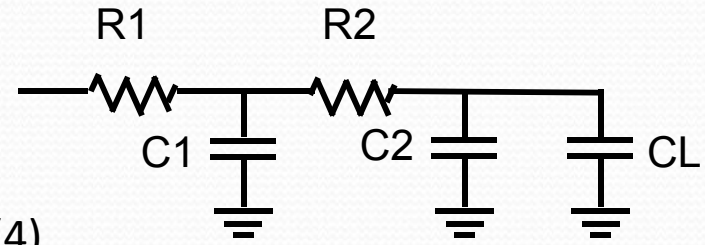
$$a_3 m_1^{\,3} + a_2 m_1^{\,2} + a_1 m_1 + a_0 = 0$$

which has closed form solution.

Net Model: compute R's and C's

- R1, and R2 are computed from m1 and m2 with C1 + C2 = C_total

$$\begin{cases} -R_1(C_1+C_2+C_L)-R_2(C_2+C_L)=m_1 \\ -R_1R_2C_1(C_2+C_L)+m_1^{\,2}=m_2 \end{cases} \quad (4)$$



- In the absence of positive solutions for R's and C's, solve the Least Square problem.

$$\min \quad [m_1+R_1(C_1+C_2+C_L)+R_2(C_2+C_L)]^2+[m_2+R_1R_2C_1(C_2+C_L)-m_1^{\,2}]^2$$

$$\text{s. t.} \quad R_1,R_2,C_1,C_2>0$$

Gate Delay/Slew Based on Net Model

- Find new Ceff based on net model

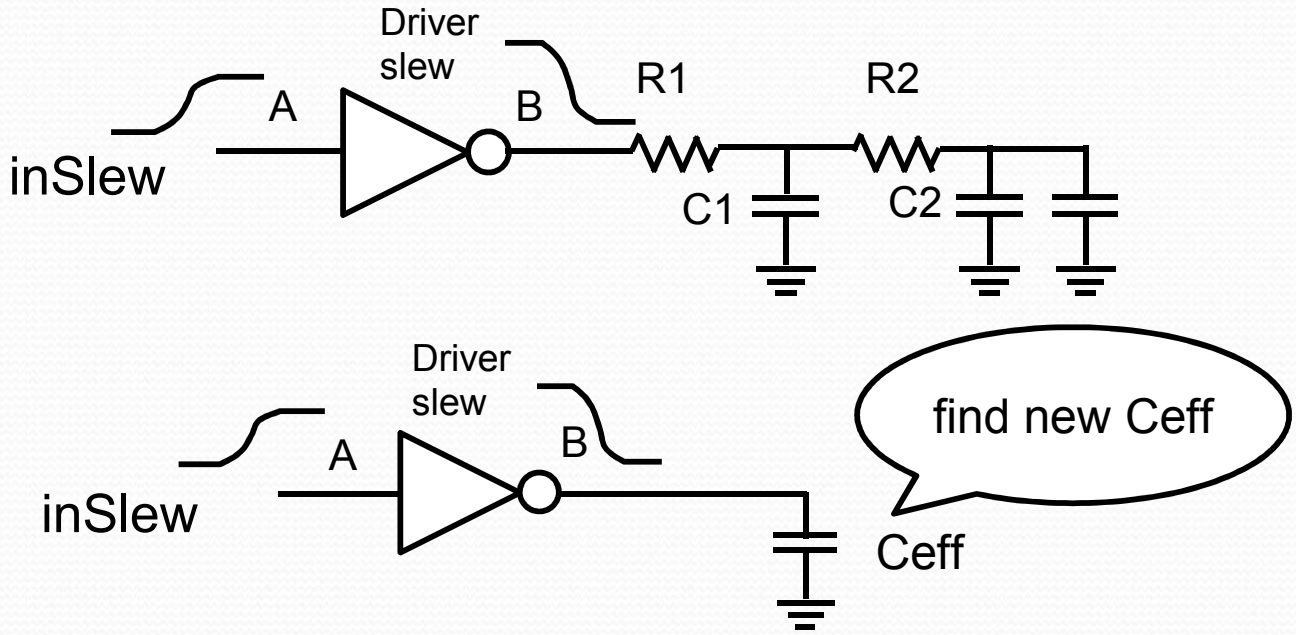


Figure 3: gate driving ceff or net delay model

Extension to Current Source Model

- Modifications to handle CSM
  - The interconnect net models are derived from the initial timing results of CSM reference timer.
  - For the receiver model, the average of two receiver capacances is used as load cap (C_L in Figure 2).

Experimental Results

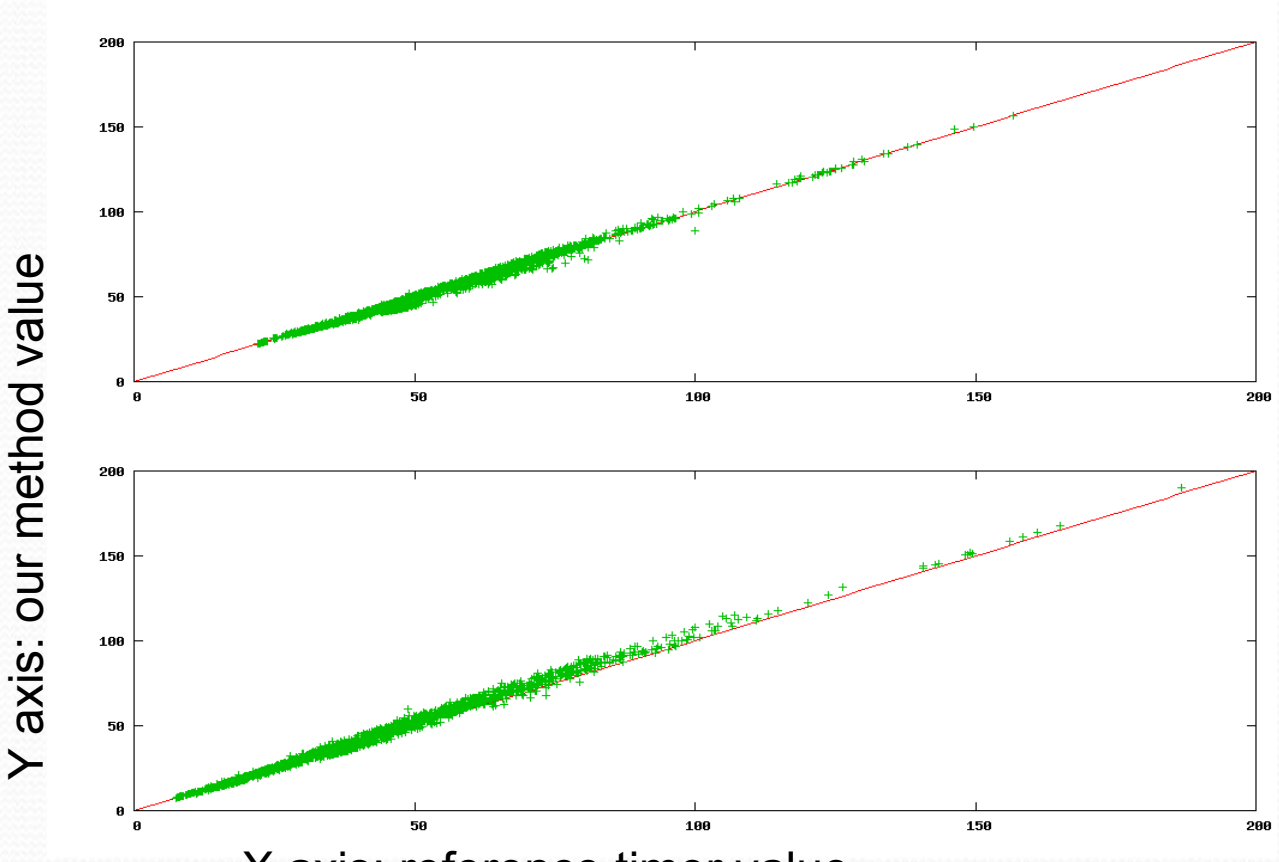
- The presented method is implemented in our in-house tool.
- Benchmarked 4 design blocks

  Number of Gates : 35K ~ 730K

  Number of Nets : 36K ~ 789K

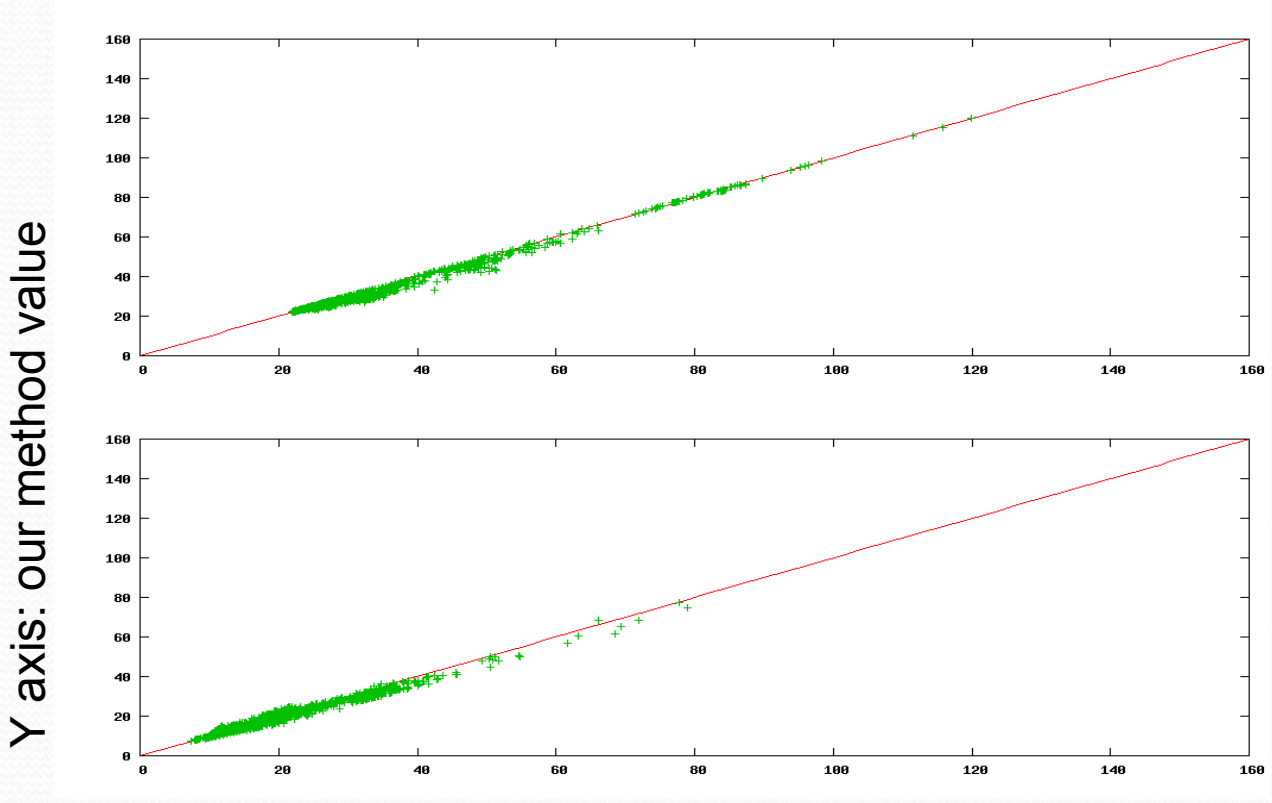
  Technology Node : TSMC 20nm.

Figure 4: NLDM delays and slews of net correlation with reference timer



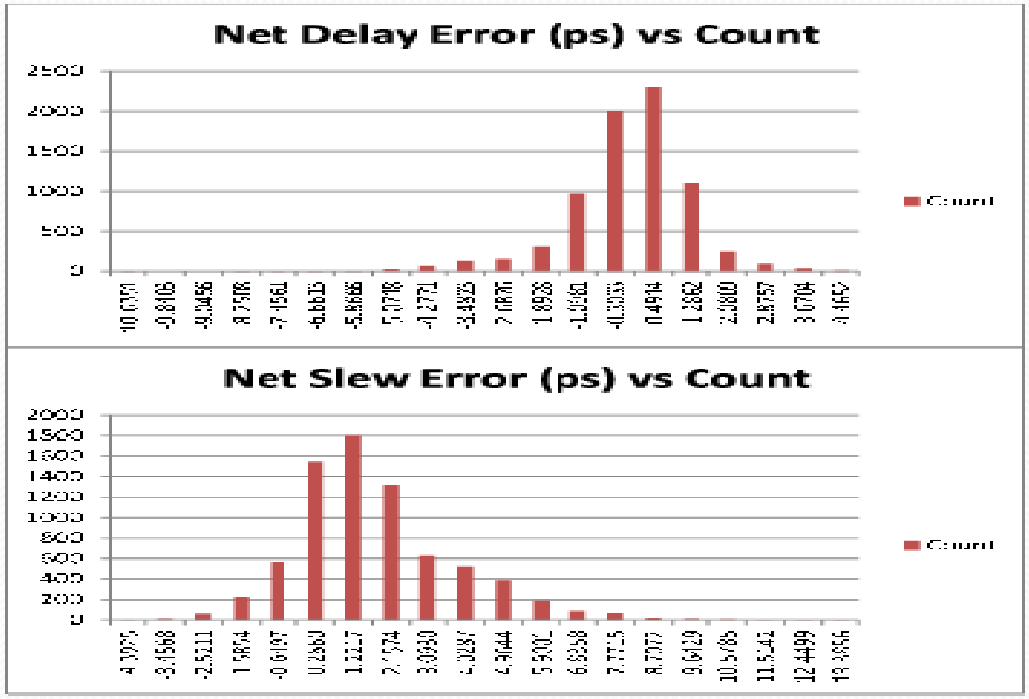
Top : net delay comparison between reference timer and our method
bottom: net slew comparison between reference timer and our method

Figure 5: NLDM delays and slews of gate correlation with reference timer



Top : gate delay comparison between reference timer and our method
bottom: gate slew comparison between reference timer and our method

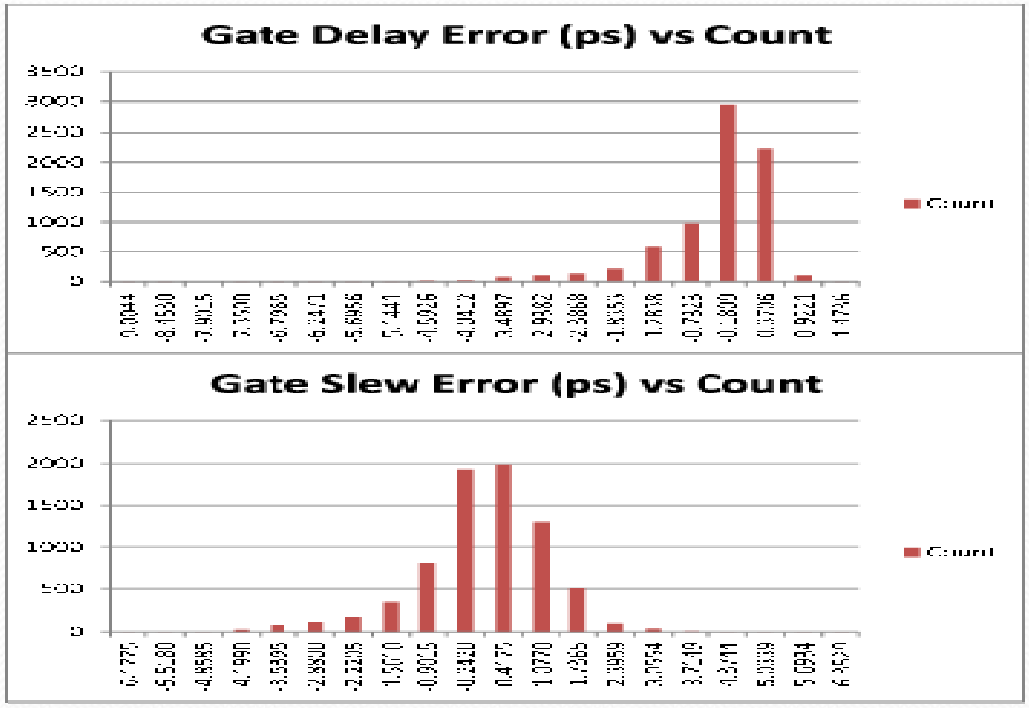
Figure 6: NLDM delay and slew error distribution for nets



Y axis: count

X axis: Error (ps) vs reference timer

Figure 7: NLDM delay and slew error distribution for gates



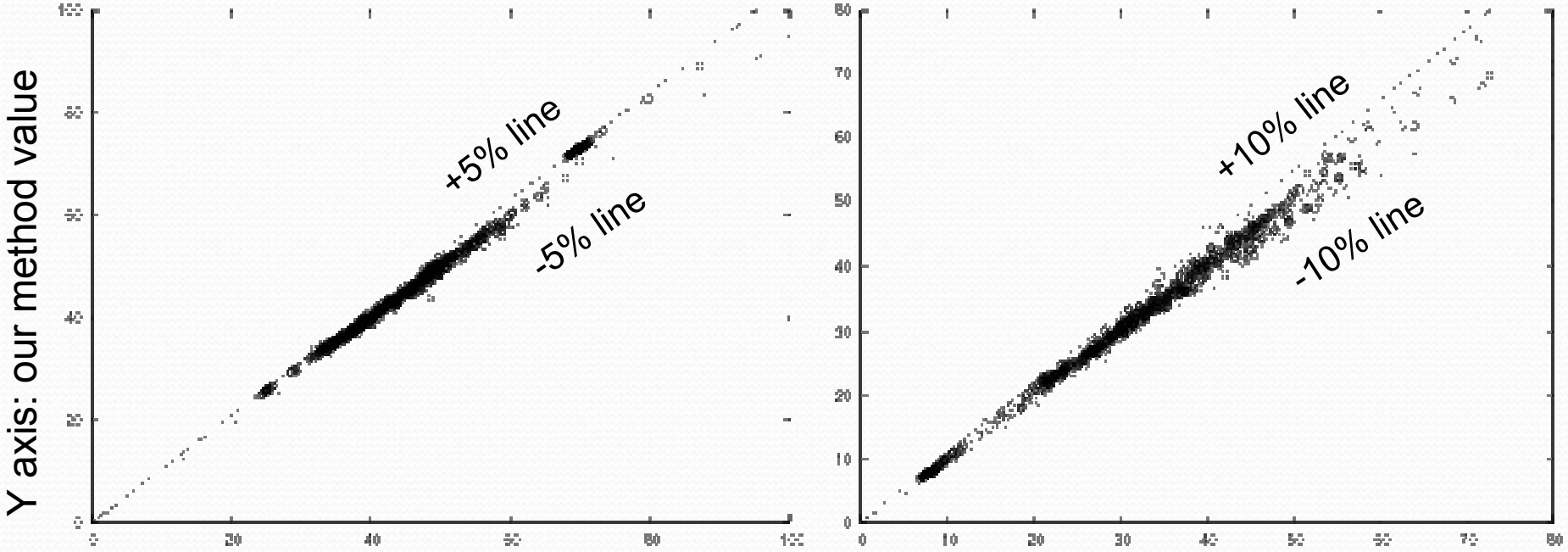
Y axis: count

X axis: Error (ps) vs reference timer

Table 1: average and max diff. of NLDM delays and slews w. r. t. reference timer, and memory save.

designs	net delay		net slew		gate delay		gate slew		Mem w. Para (MB)	Mem w/o Para (MB)	Mem save (%)
	Ave. diff(ps)	Max diff(%)	Ave. diff(ps)	Max diff(%)	Ave. diff(ps)	Max diff(%)	Ave. diff(ps)	Max diff(%)			
d1	0.523	8.39	0.415	10.44	-0.535	9.98	0.537	17.85	1060	447	57.8%
d2	0.0342	9.75	0.229	14.31	0.435	12.19	0.151	17.01	5739	836	85.4%
d3	0.736	8.82	0.964	15.74	0.931	14.33	0.43	19.90	2823	1108	60.8%
d4	-0.0247	9.99	0.953	16.42	-0.298	16.45	-0.0211	19.81	4234	1452	65.7%

Figure 8: CSM stage delays and slews of net and gate correlation with reference timer



Left : stage delay comparison between referene timer and our method. Most are within +-5% lines

Right : gate slew comparison between reference timer and our method. Most are within +-10% lines

Conclusion

- A new approach to estimate delay and slew without explicit parasitic data is presented and implemented.
- Excellent accuracy with this fast computation method has been established by qualifying on many designs and comparing the timing results with reference timer.

References

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