KYOTO INSTITUTE OF TECHNOLOGY

Transistor Size Optimization Methodology for Logic Circuits Considering Variations caused by BTI and Process

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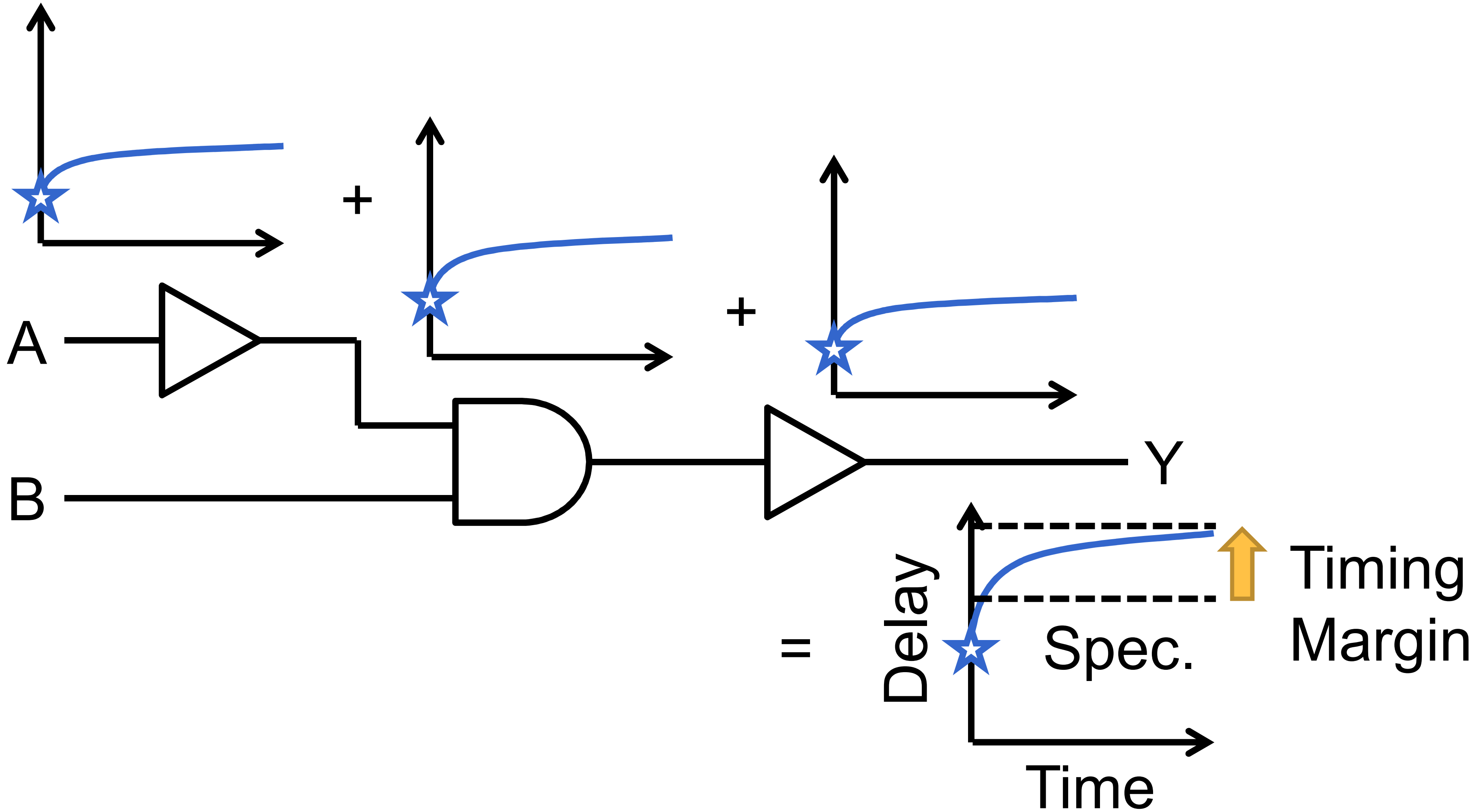
Summary

Transistor Size Optimization Technique

- BTI (Bias Temperature Instability) and process variations into consideration
- Lifetime delay of logic path – 4.4% reduced ☺
- Area – no overhead ☺
- # of cells in library – 3x~ ☹

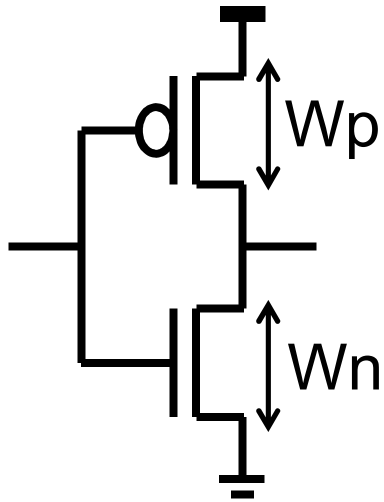
Background – Aging Degradation

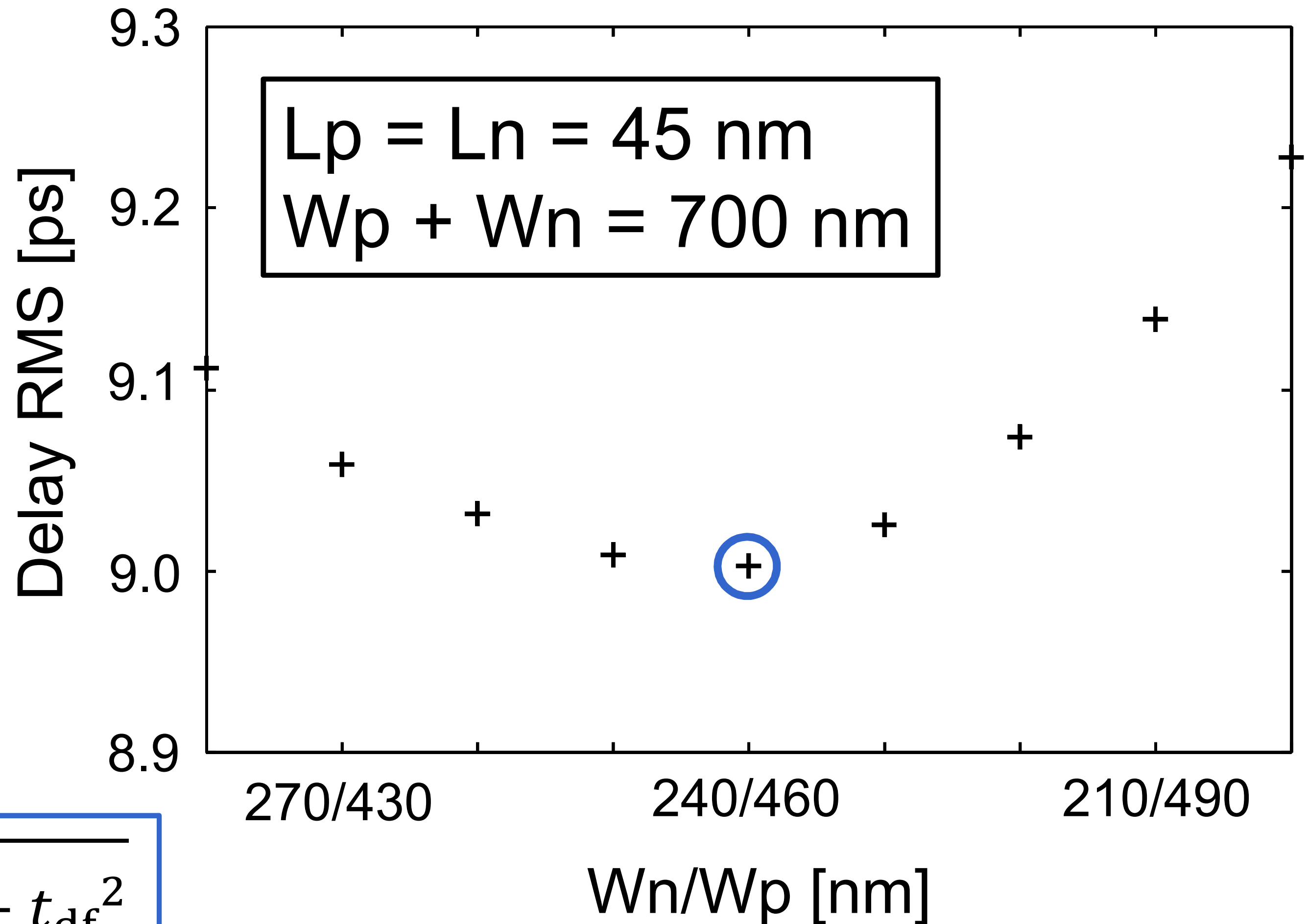


Scaling – increase aging degradation

Prediction and compensation – INDISPENSABLE

Transistor Size Optimization

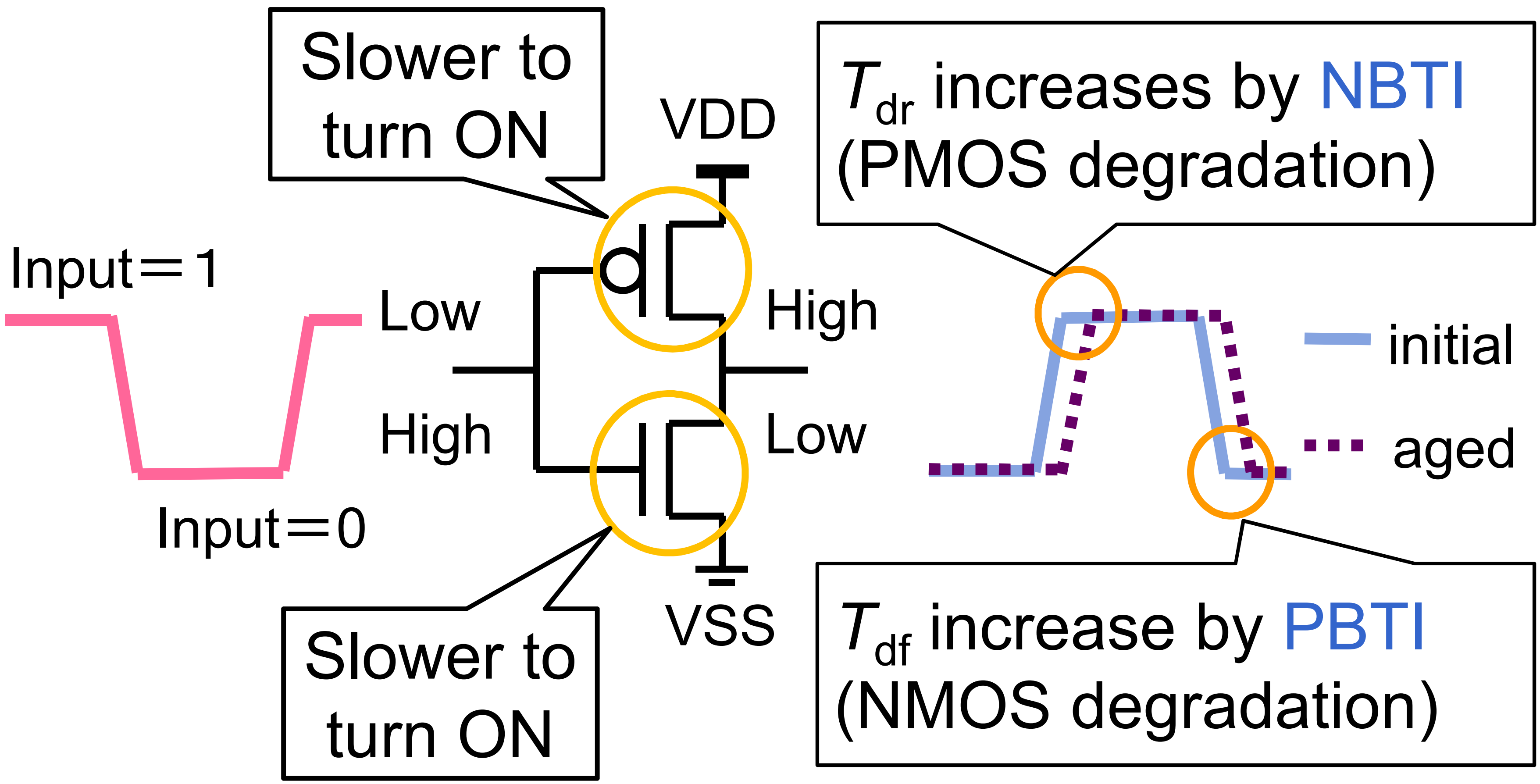




$$d_{\mathrm{RMS}} = \sqrt{\frac{{t_{\mathrm{dr}}}^2 + {t_{\mathrm{df}}}^2}{2}}$$

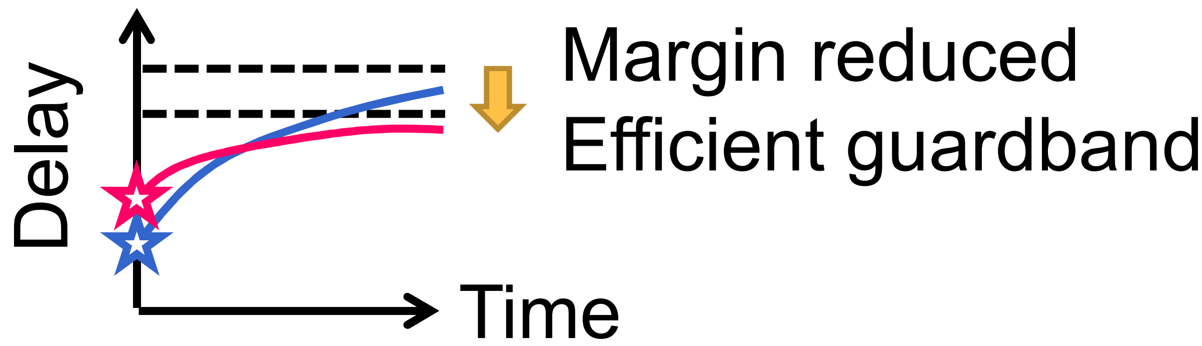
- Conventional – initial delay based

Impact of BTI on Inverter



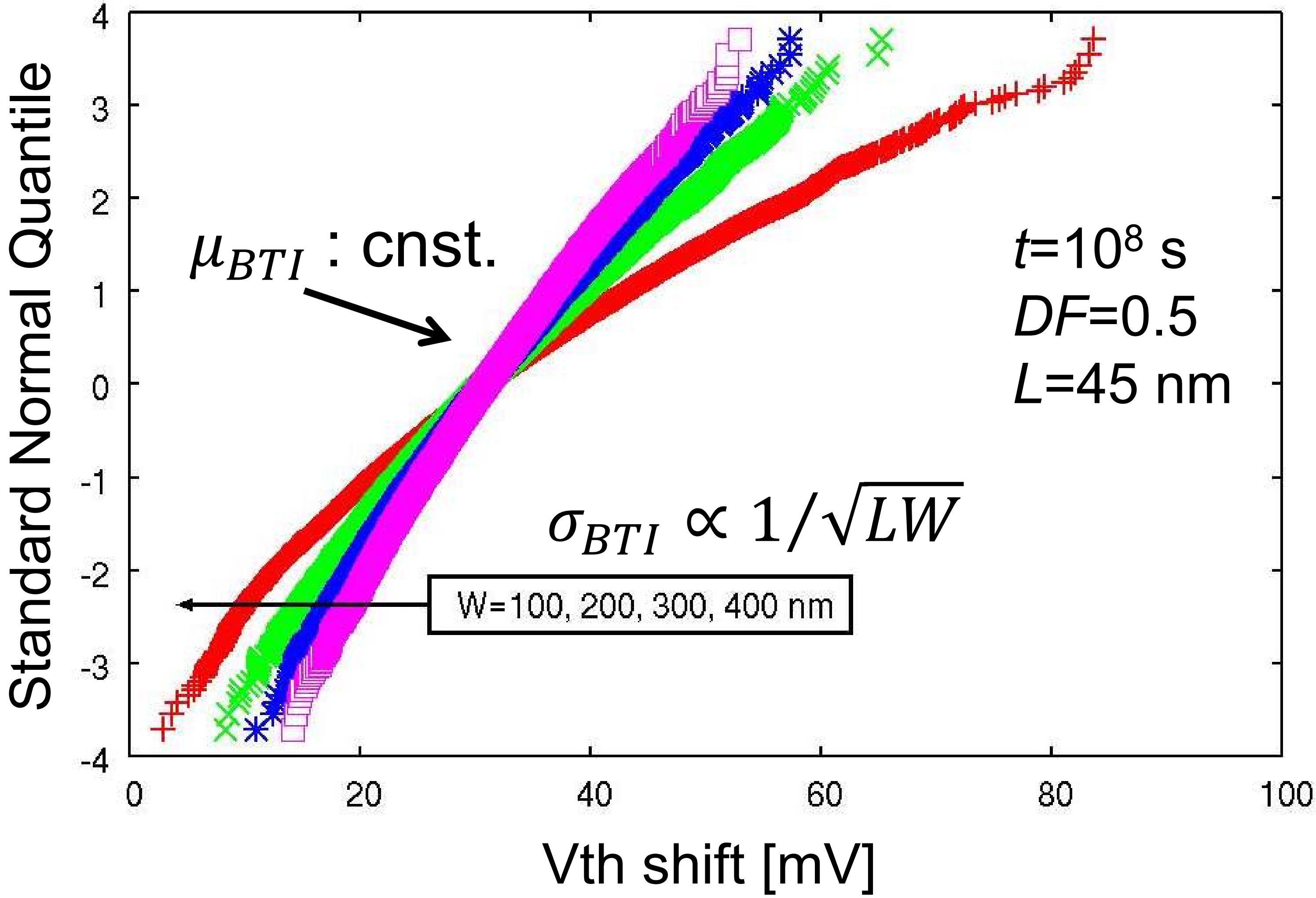
- Since 45 nm process – Both BTI
- Imbalance – T_{dr} and T_{df} degradation

Purpose of This Study



- Propose – lifetime delay based
- Key ideas
  - Consider "lifetime experience" in logic gate design
  - Optimize transistor size to reduce "BTI-induced variation"
- Design cells for DF (Duty Factor) = 0, 0.5, 1

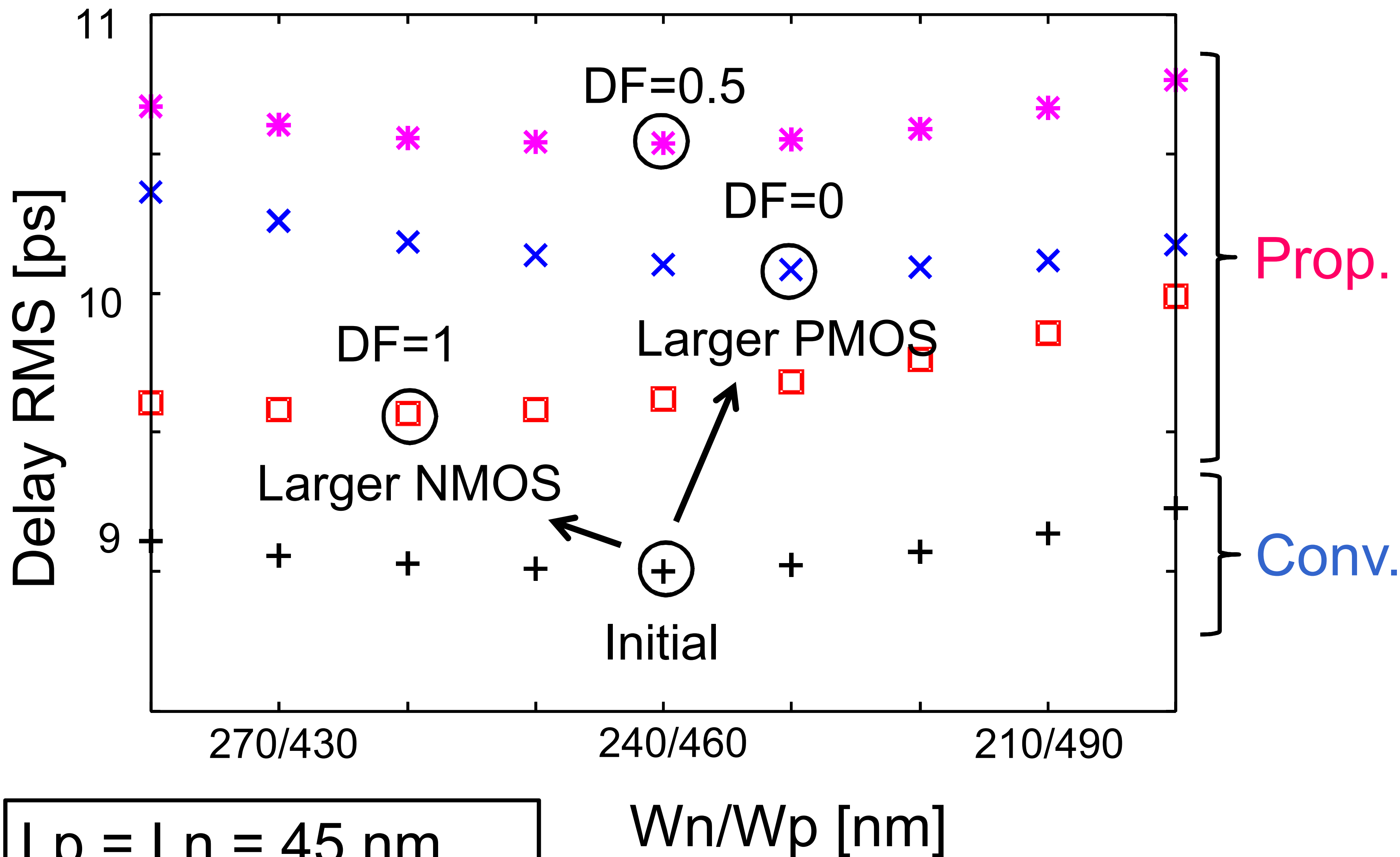
Sizing – BTI-Induced Variation



- Enlarge transistor size – reduce BTI variation

Kobayashi Lab.

Results of Size Optimization

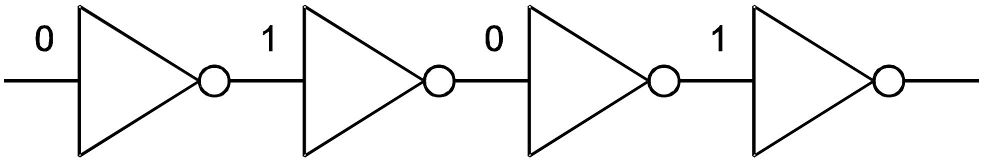


Lp = Ln = 45 nm
Wp + Wn = 700 nm

Simulation Result – INV Chain

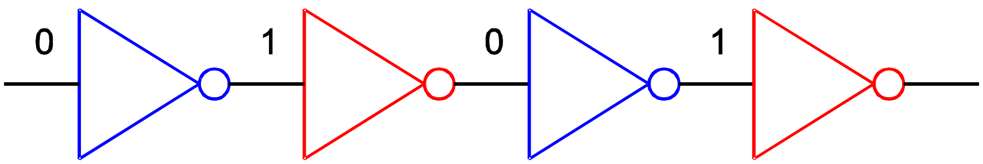
4.4% ☺

Conventional (initial based)

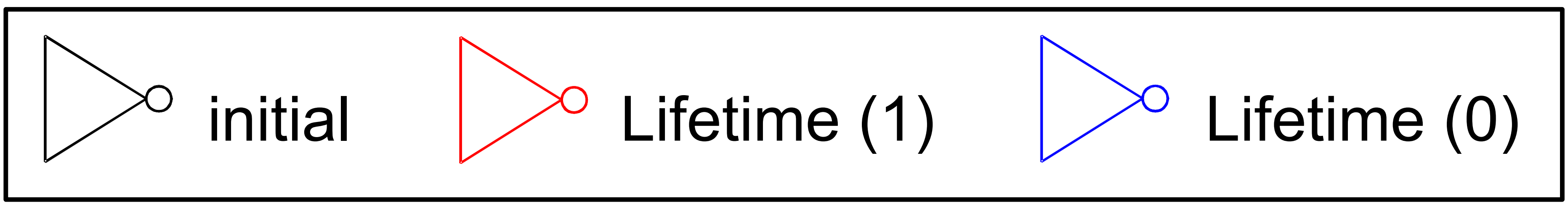


Initial: 64.8 ps
Lifetime: 76.6 ps

Proposed (lifetime based)



Initial: 66.5 ps
Lifetime: 73.2 ps



- Lifetime delay – improved w/o area overhead

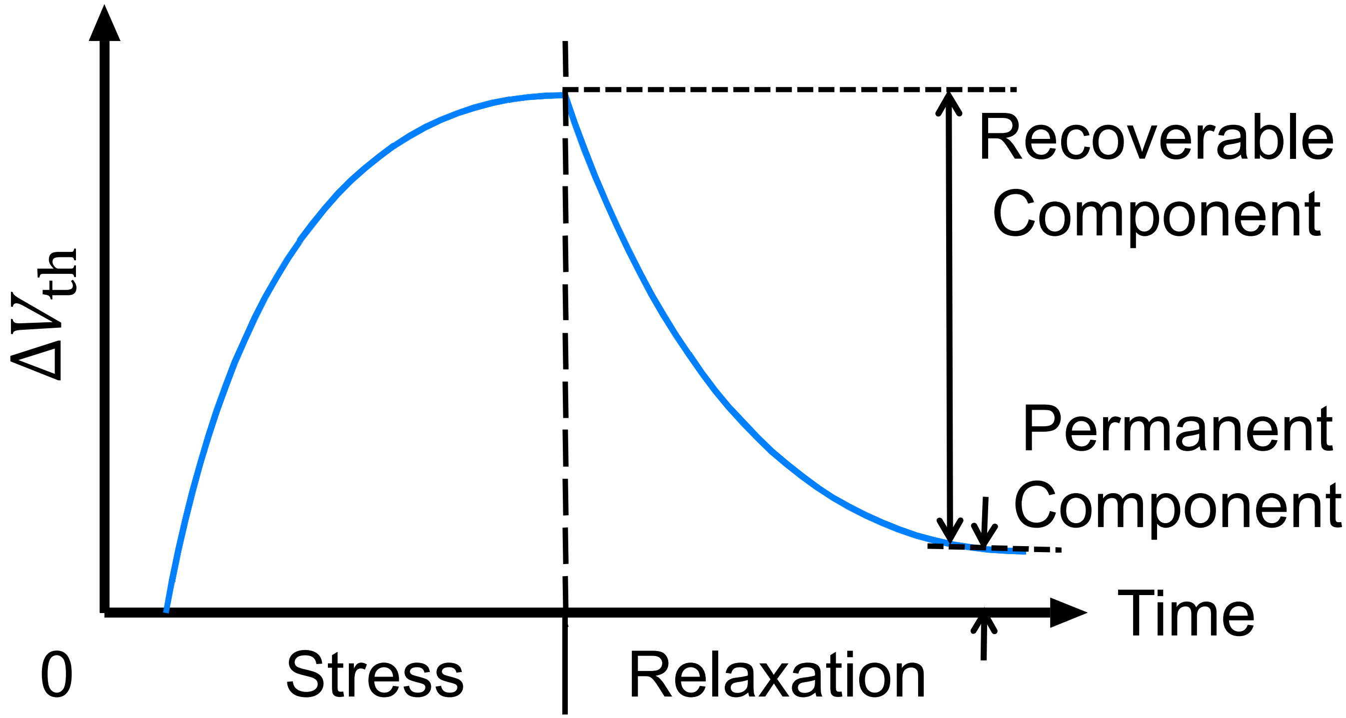
Conclusion

- Transistor size optimization technique
  – Conventional – initial delay based
  – Lead to large timing margin

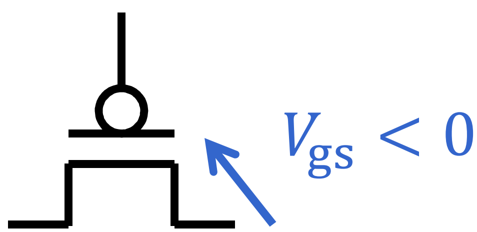
  – Proposed – lifetime delay based
  – Path delay of inverter chain – improved by 4.4%
  – No requirement of area overhead
  – Support dependable and efficient chip designs

Thank you for listening!

BTI (Bias Temperature Instability)

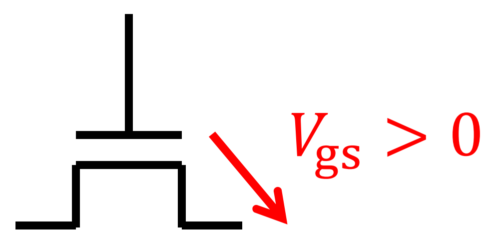


NBTI (Negative BTI) on PMOS



65 nm~

PBTI (Positive BTI) on NMOS



40 nm HKMG~

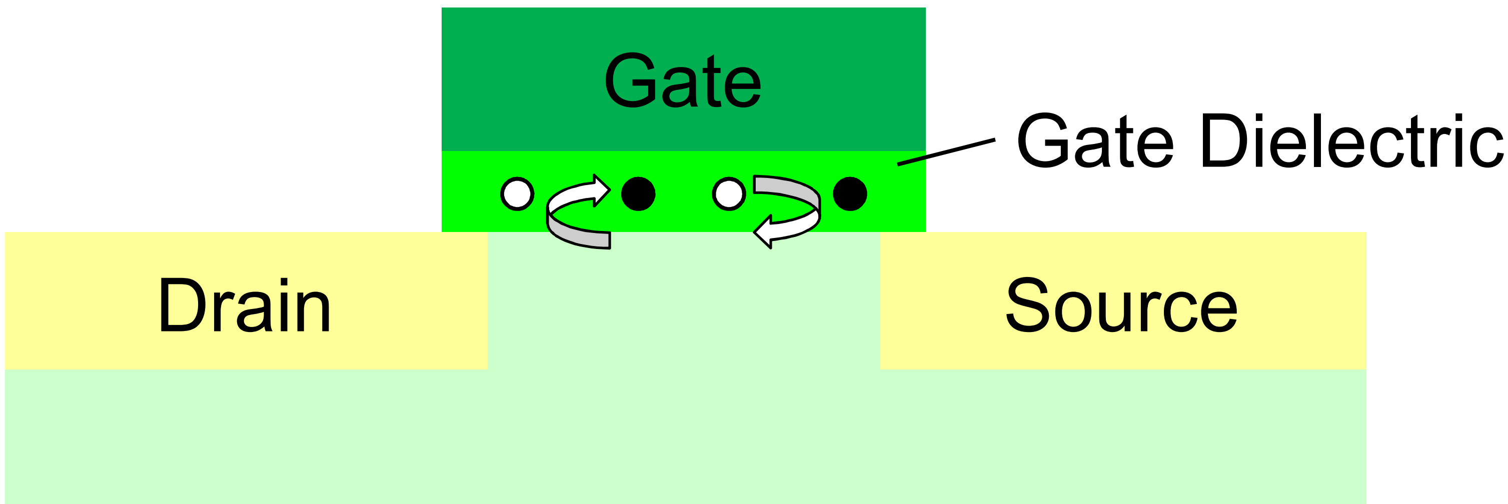
Technique to Overcome Degradation

- **Adaptive Techniques**
  - Body biasing
  - Adaptive Supply Voltage
- **Non-adaptive Techniques**
  - Sizing
  - Strengthen

- Overhead required
- Based on aging prediction

Physics – Atomistic Trap-Based Model

AT-B Model



● : Defect (capture) ○ : Defect (emission)

- Defect – capture and emit carriers

Calculate ΔV_{th} Distribution by BTI

Defect-centric distribution

Input: transistor size, stress condition

Product of Nt and η

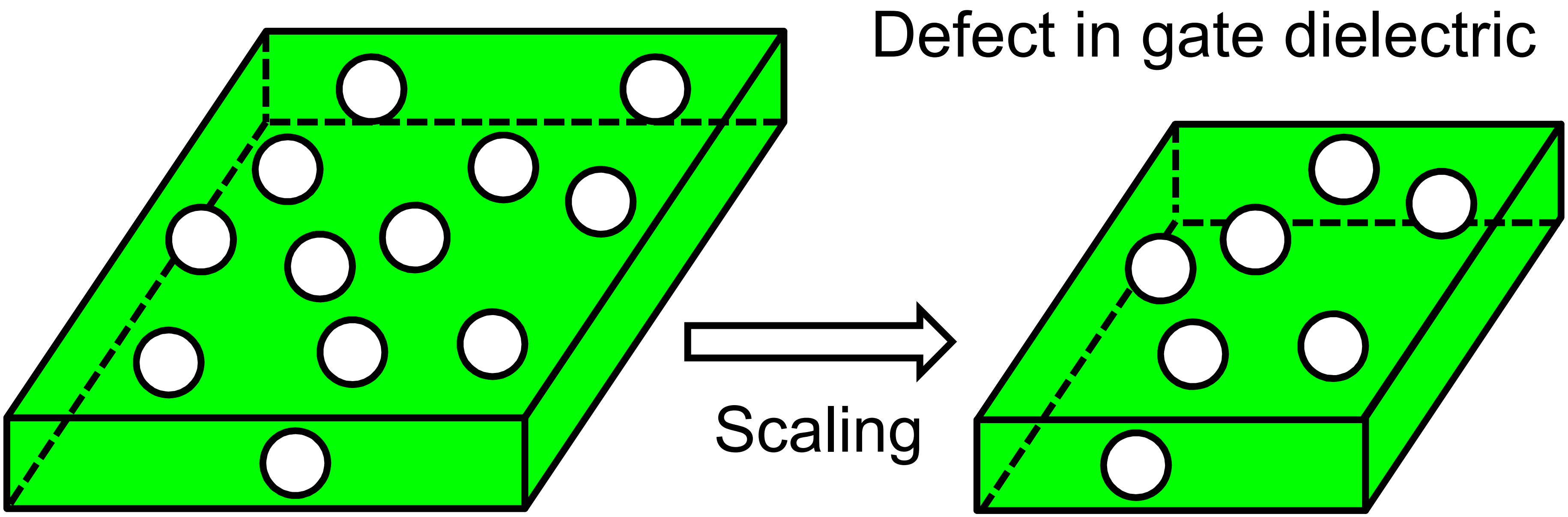
Nt: number of defect (Poisson dist.)

η: impact of single defect (Exp. Dist.)

Output: ΔV_{th}

P. Weckx et al., IRPS 2014

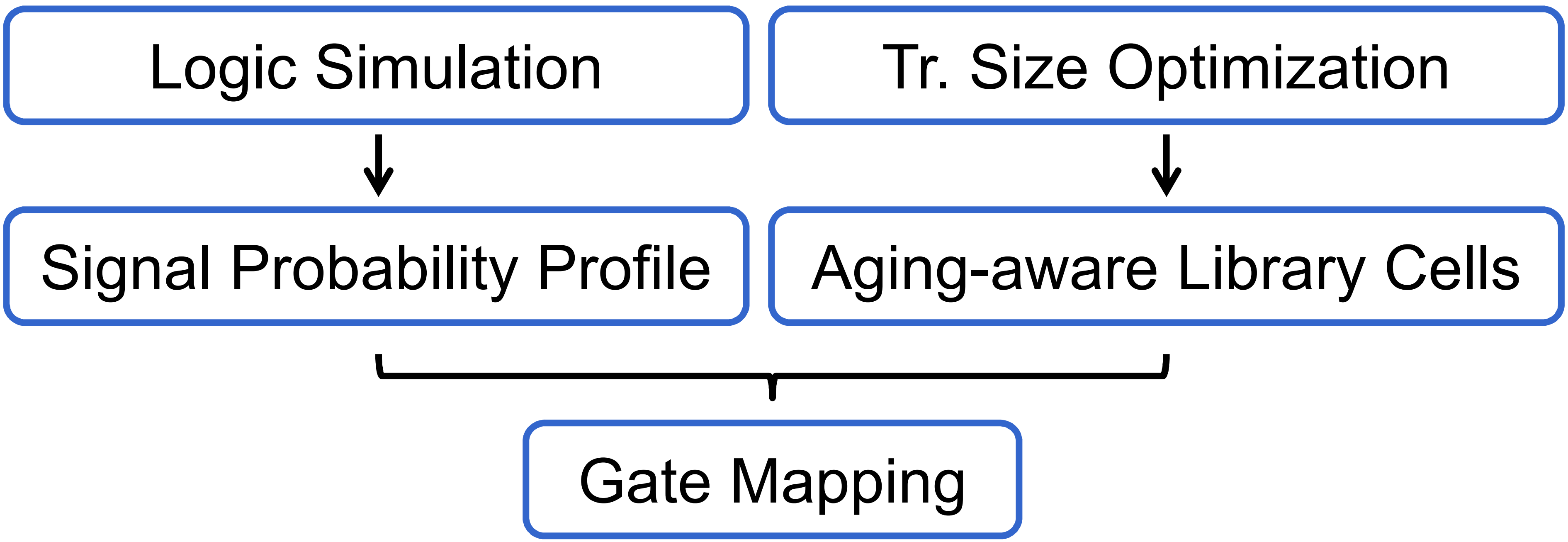
Physics – Scaling of BTI



Number of defect – decrease ↓
Impact of single defect – increase ↑

- Average μ_{BTI} – constant
- Deviation σ_{BTI} – area dependent ($\propto 1/\sqrt{LW}$)

Aging-aware Library



Optimization for Multi-input Gate