Timing Interoperability in the Age Of Silos

Panelists

- Florin Dartu – TSMC
- Ruben Molina – Cadence
- Paul Penzes – Qualcomm
- Vasant Rao – IBM
- Jim Sproch – Synopsys

Outline

- Do we have timing interoperability? – not just between timing tools, but across all tools that use/consume timing the flow
- Is timing interoperability important?
  - Virtue or vice?
  - What advantages/disadvantages accrue with each approach?
  - What is the role of standards?
- What is the best way forward?

Florentin Dartu

- Florentin Dartu is a Deputy Director at TSMC, leading a small team in charge of LVF library deliveries to customers, certifying STA tools, evaluating sign-off methodologies, and generally coercing EDA providers to work together in the timing sign-off area. Before joining TSMC in 2013, he attempted to make a difference in the PrimeTime team (hierarchical STA, CRPR, POCV). Earlier than that, he spent many years at Intel and Synopsys research labs working on circuit simulation, STA delay engines and SI analysis.

Ruben Molina

- Ruben Molina serves as the Director of Product Marketing for Digital Timing Signoff at Cadence. He is responsible for setting product rollout strategy, and establishing tool requirements and roadmaps. Prior to Cadence, Ruben held marketing and technical management positions in timing analysis and signoff methodology at Magma Design Automation, Extreme DA and LSI Logic. Ruben holds a BS in Engineering and an MSEE from California State University, Los Angeles.

Paul Penzes

- Paul Penzes is a Senior Director of Engineering at Qualcomm. As the lead of the Design Technology (DTECH) team, he manages the timing, PPA R&D, testchip and design technology integration teams within the Central Engineering and Technology organization. Before Qualcomm, Paul was an Associate Technical Director and Distinguished Engineer at Broadcom, and prior to that a Senior VLSI Engineer and Myricom. Paul has 19 patents issued, 14 pending, and has a B.S., an M.S. and a Ph.D in Computer Science from the California Institute of Technology, Pasadena.

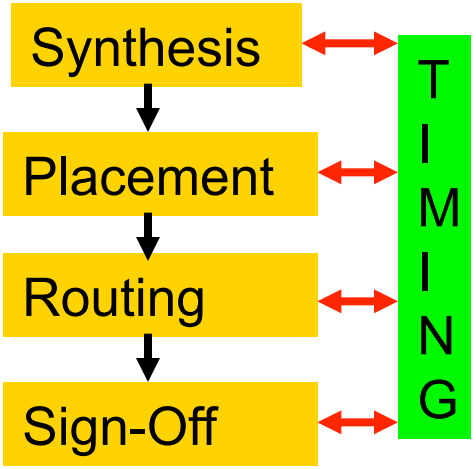
Vasant Rao

- Vasant Rao is currently a Senior Technical Staff Member at IBM Systems in Poughkeepsie, NY. During his 25 years at IBM, he has worked in several areas. Currently, his interests include Statistical Static Timing Analysis (both Gate and Transistor Level), Library Characterization, Circuit Extraction and Simulation. He has 7 patents granted, 9 pending and has published over 50 papers.

Jim Sproch

- Jim Sproch is a Senior Director of R&D at Synopsys, where he is currently responsible for transistor-level static timing analysis, transistor-level equivalence verification, and library tools. In the past he has been responsible for other EDA product families at Synopsys including low-power synthesis/optimization, DFT, ATPG, and library characterization. Jim is currently chair of the Liberty Technical Advisory Board, and he was a primary contributor to the UPF / IEEE 1801 series of power intent standards. He joined Synopsys from Standard Microsystems Corporation, where he designed and implemented advanced VLSI chips for networking, graphics, magnetic disk, and peripheral controllers. Jim received a B.S. in Electrical Engineering from Rensselaer Polytechnic Institute, he holds twelve issued U.S. patents, and has published several technical papers in the domain of semiconductor electronic design

Tool Interoperability



- Besides Sign-Off, Static Timing Engine is tightly integrated into Physical Design and Construction Tools.
- Interoperability at Sign-Off level is easier to achieve.
  - Not a “slam-dunk” though considering Timing influence on Noise, Power, and EM.
- But much harder at the integrated level
  - Given a silo from company A, can we replace its Router with a better one from company B?
  - Need to define very strict standards/hooks that all EDA Vendors must adhere to.
  - Holy Grail/Nirvana from an EDA Customer point of view.

Virtue or Vice

- EDA Customer
  - Huge Virtue, especially if Nirvana (previous slide) can be achieved.
  - Better flexibility for mix-and-match.
    - Improved Design Quality
    - Less $$ on tool integration
  - No single vendor is best in all tools
    - Company A may have the world's best Synthesis and Placement Tool while Company B has the best Router
- EDA Vendor
  - Virtue
    - Forces competitiveness. If you are not good enough, you are out.
    - Better chance for a New player to get in with some specific innovative process or tool.
      - Don't need to wait for getting bought by an existing Big player and get incorporated into their silo.
      - Silos drive industry consolidation which hinders innovation/cost/flexibility.
    - Widens customer base. You now have a shot at a customer who has been traditionally using a "silo" from another vendor.
  - Vice
    - Cannot bank on financial advantage of "Silos".
    - Easier for customer to benchmark your tool vs competitor's tool.
    - Adhering to "standards" may hinder
      - quality?
      - innovation?

Panelist: Jim Sproch

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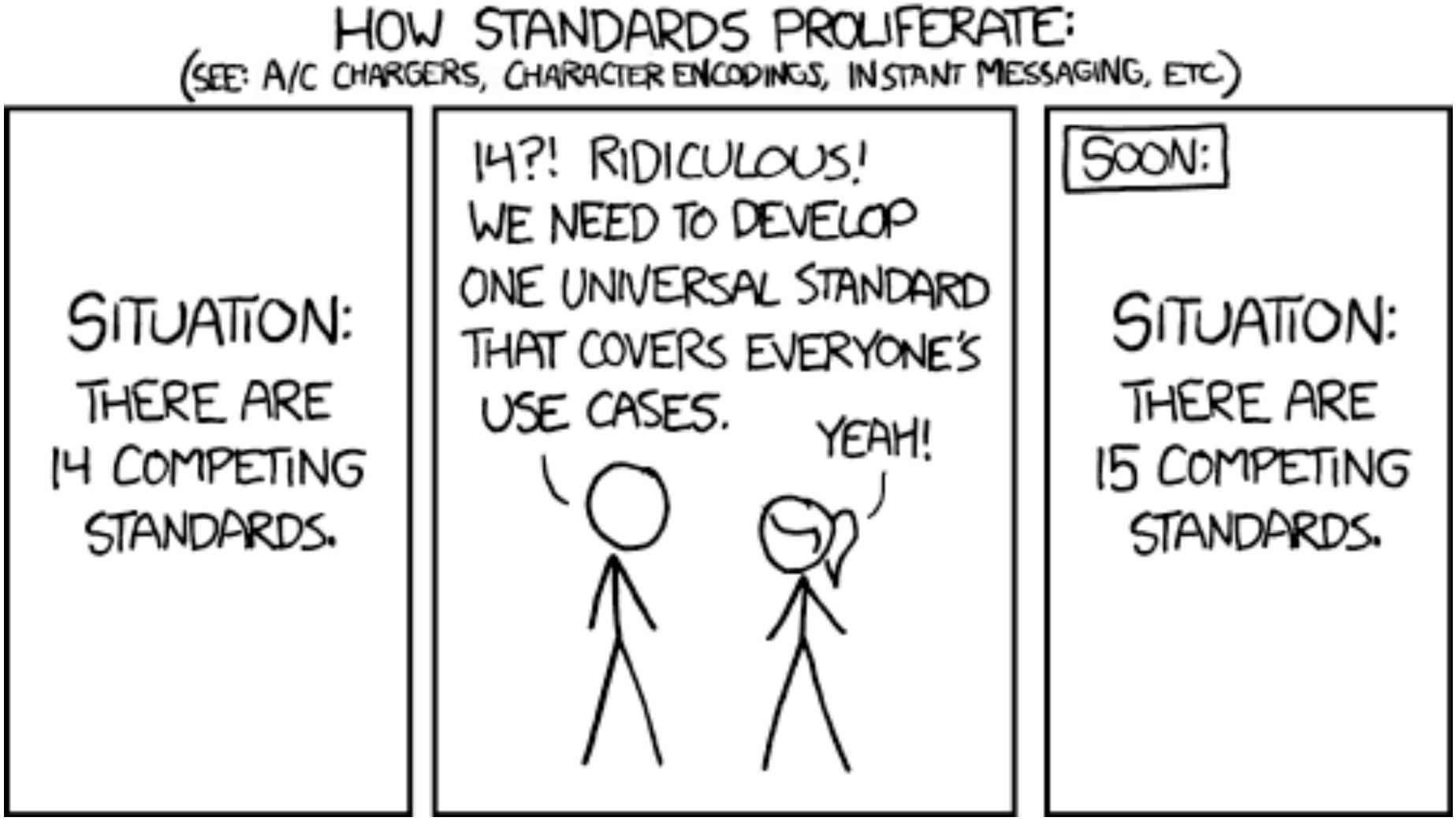
Reality Check

Source: XKCD



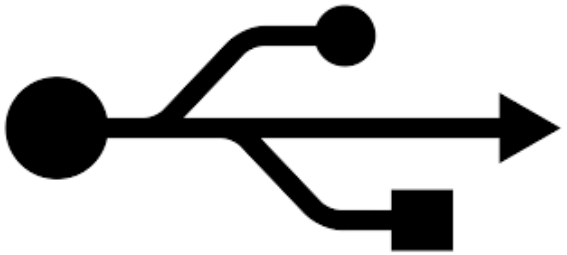
Standards: What are they good for?

- The good thing about standards: there are so many to choose from.
- The best thing about standards: everybody has their own.
- Standards provide
  - Interoperability
  - Efficiency by reducing duplication and distractions
- Better to know what standards are *not* good for
  - Innovation
  - Differentiation
  - Rapid evolution
  - Building a monopoly
  - Generating massive profits

What's the difference between USA and USB?

- One connects to all of your devices and accesses your data.

- The other is a hardware standard.



Source: twitter @alfiedotwtf

A Well-Known Timing Standard

- Liberty is a standard for library cell data modeling
  - Open source standard, with LTAB
  - Operated under the auspices of IEEE-ISTO
  - Timing, Noise, Power, Variation, etc.
  - Language semantics, not tool semantics
  - Decades of successfully delivering EDA tool interoperability
  - Stable, scalable, straight-forward, user-extensible

- How could it be better?
  - More/less language semantics
  - More/less tool semantics
  - Faster/slower rate of change
  - More/less user readable/verbose
  - More examples
  - Smaller file size

Evolution of Ideas to Standards

- 100 verbal suggestions per annum
- 10 written proposals to review
- 5 ratified extensions to the Liberty standard

Personal Position Statement

1. Premature standardization may sacrifice innovation opportunities
2. Proprietary advancements are valuable to drive progress
3. Standardize only after industry consensus on best methods
4. Given the complexities and dynamics of EDA for STA, the current balance of standards and proprietary technology are reasonably balanced

What Other People Say About Liberty

- If **Liberty** means anything at all, it means the right to tell people what they do not want to hear.
- . . . life, **Liberty**, and the pursuit of happiness.
- **Liberty** has never come from the government. **Liberty** has always come from the subjects of it. The history of **Liberty** is a history of ~~resistance~~ transconductance.
- **Liberty**, Equality, Fraternity (or Liberté, égalité, fraternité)
- They who can give up essential **Liberty** to obtain a little temporary safety deserve neither **Liberty** nor safety.
- Give me **Liberty**, or Give me Death!

Source: respective famous historical authors per notes