The TAU 2016 Contest

Timing Macro Modeling

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Sponsors: acm cadence IBM SYNOPSYS

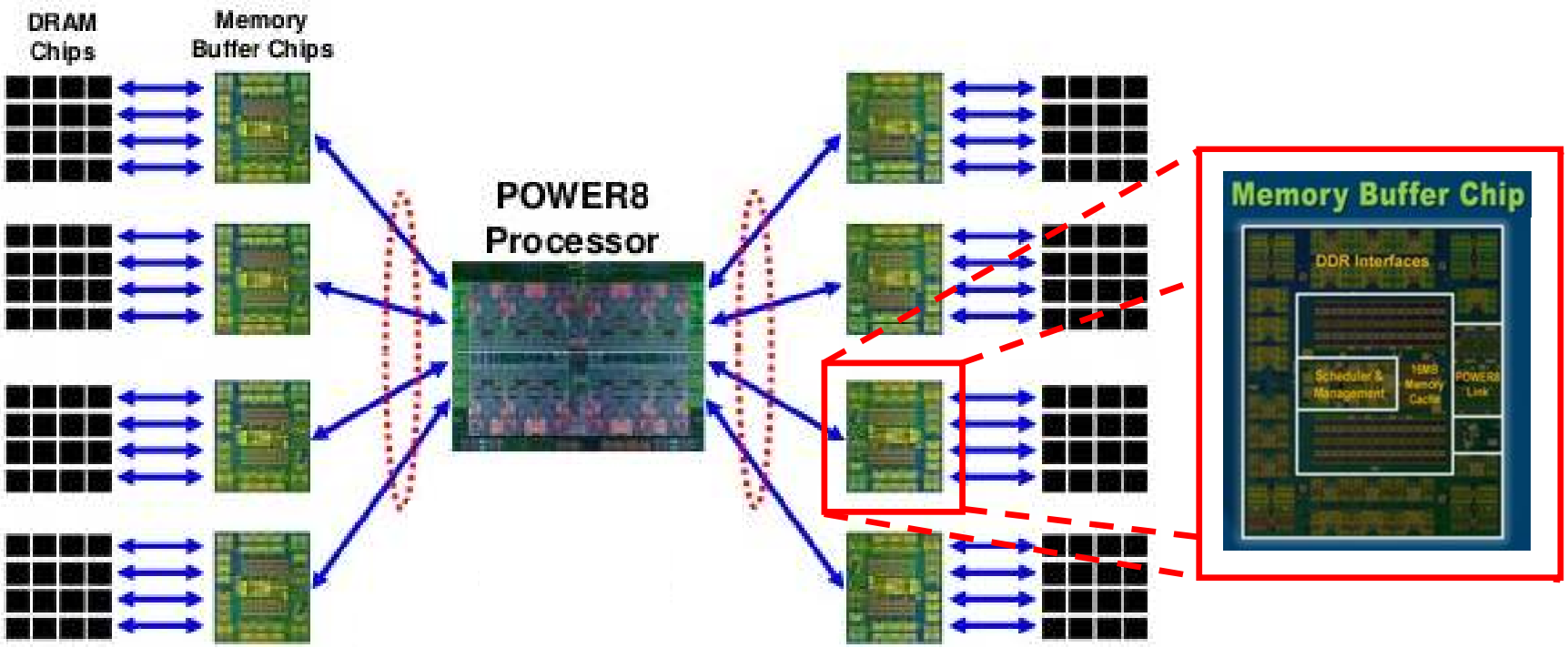
Motivation of Macro Modeling

Performance

Full-chip timing analysis can take days to complete – billions of transistors/gates

Observation: Design comprised of many of the same smaller subdesigns

Solution: Hierarchical and parallel design flow – analyze once and reuse timing models



Source: http://xtreview.com/addcomment-id-30496-view-ibm-power8-supercomputer.html

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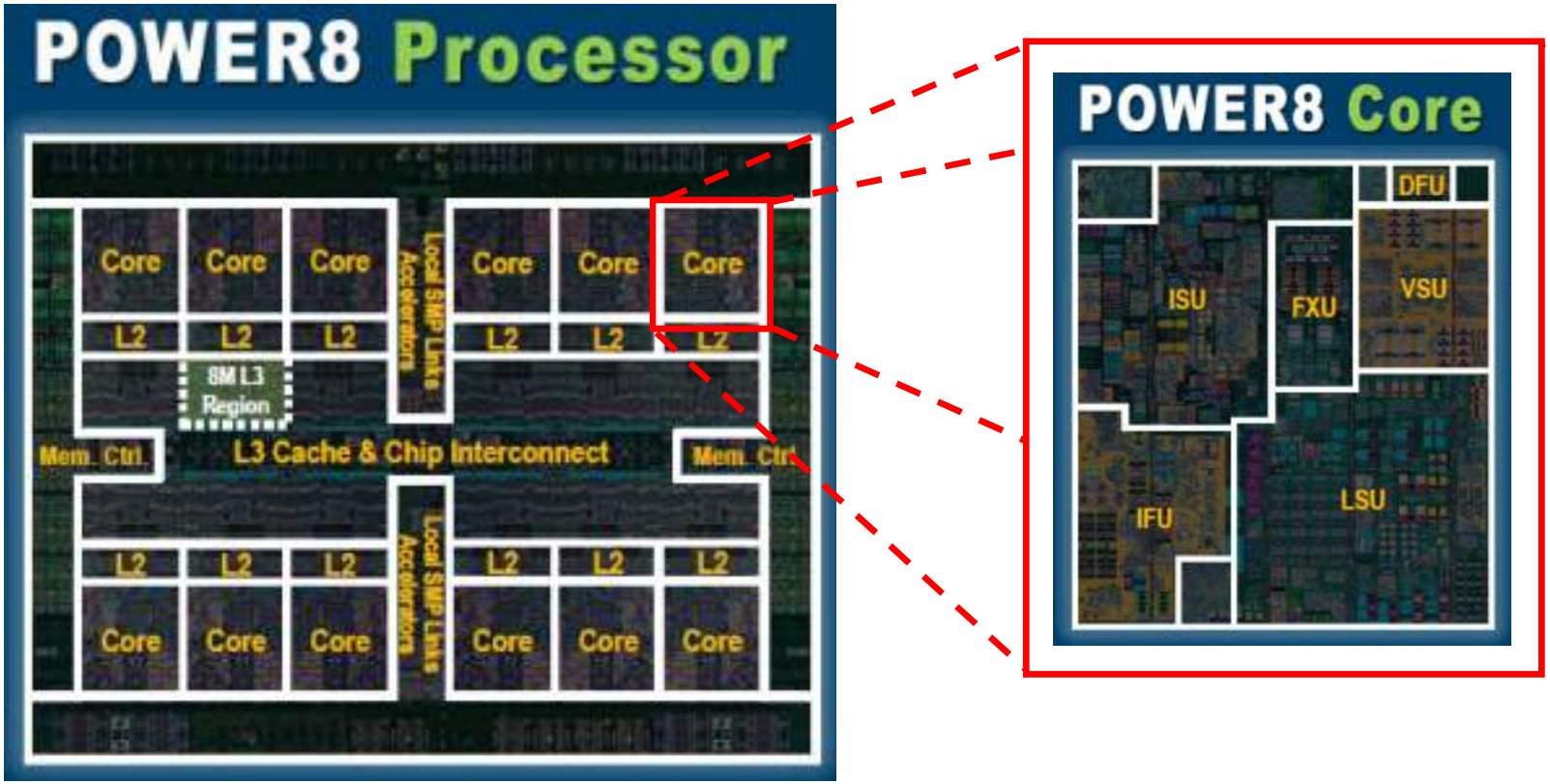

Source: http://www.cantechletter.com/2014/10/geeks-reading-list-week-october-24th-2014/
Source: http://wccftech.com/ibm-power8-processor-architecture-detailed/

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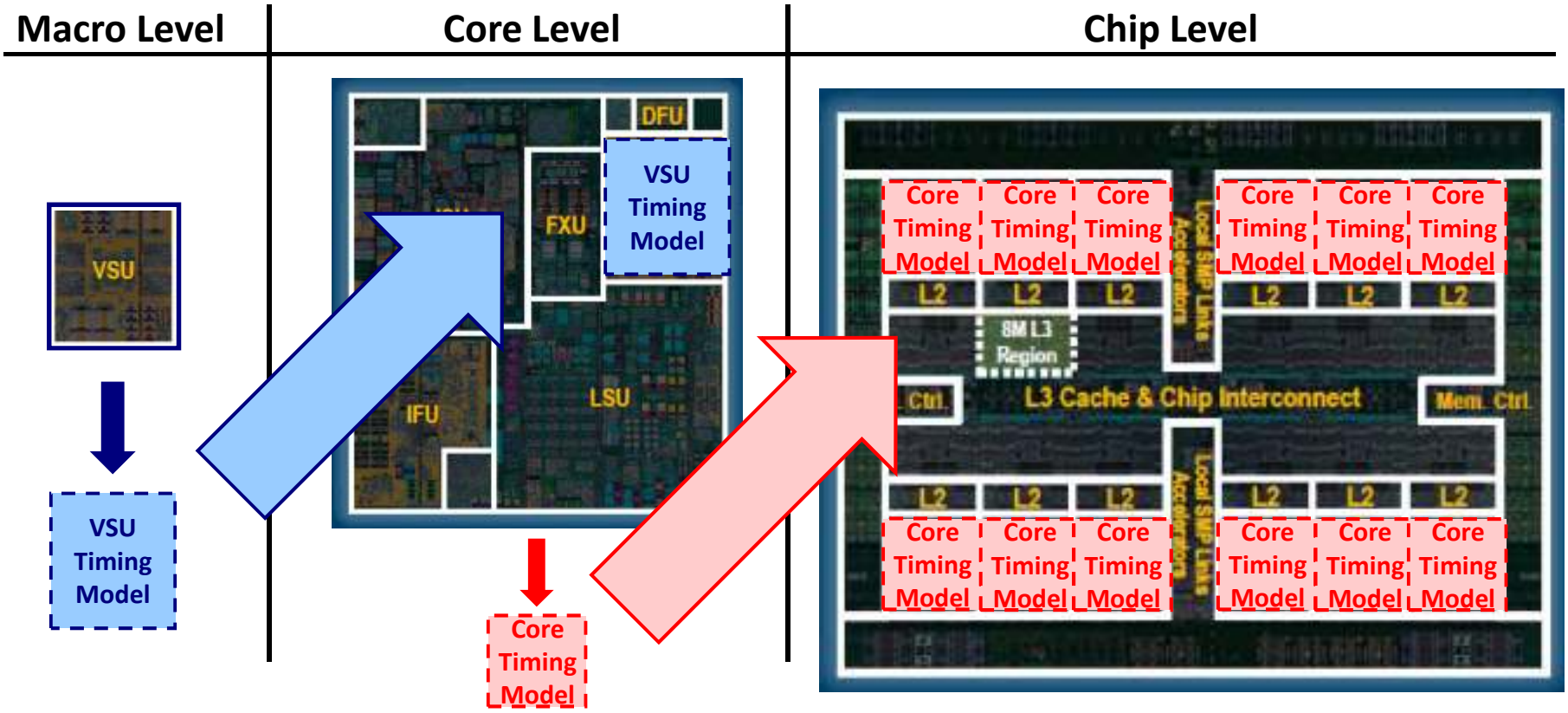


TAU 2016 Contest: Build on the Past

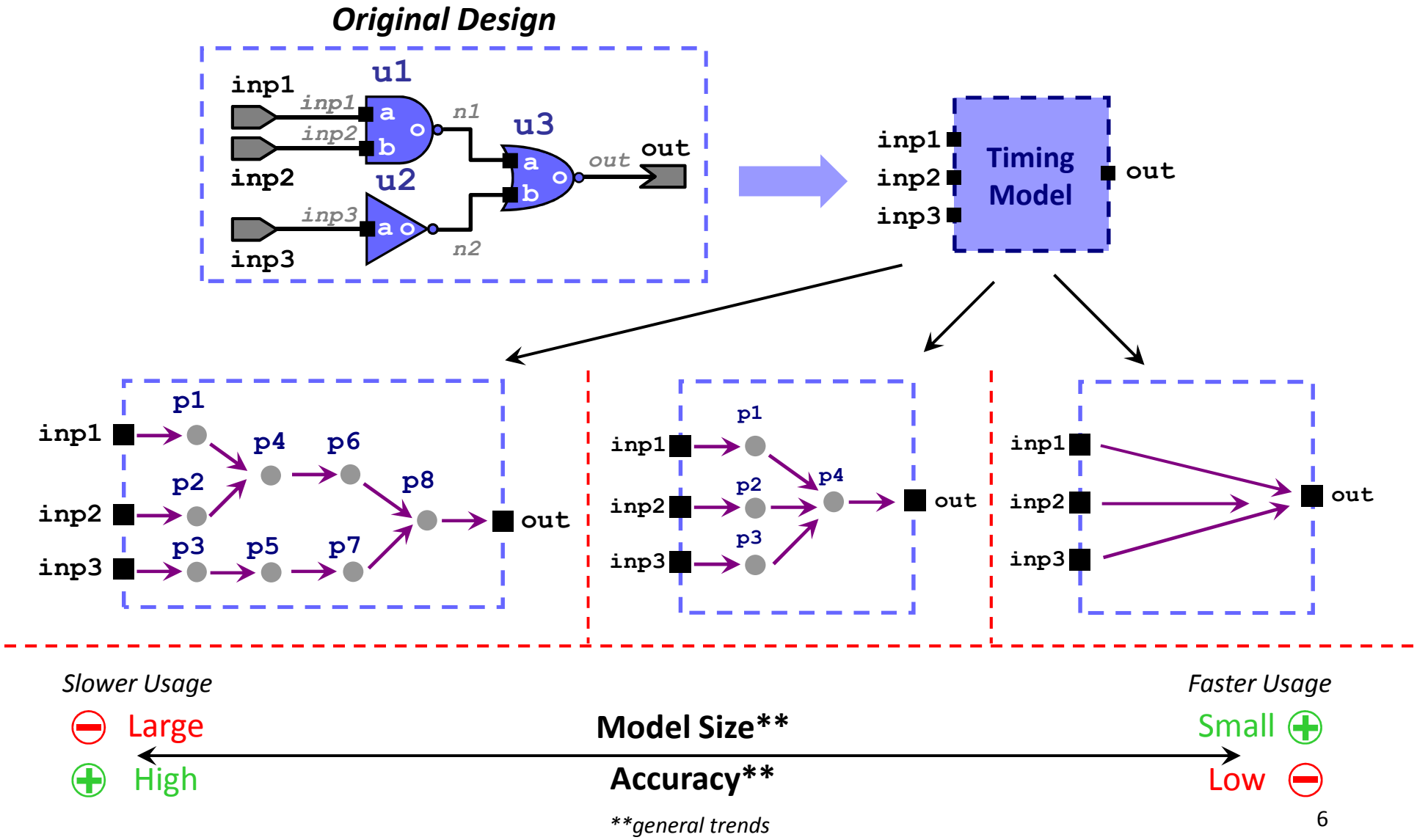
Develop a timing macro modeler with reference timer

Golden Timer: OpenTimer – top performer of TAU 2015 Contest

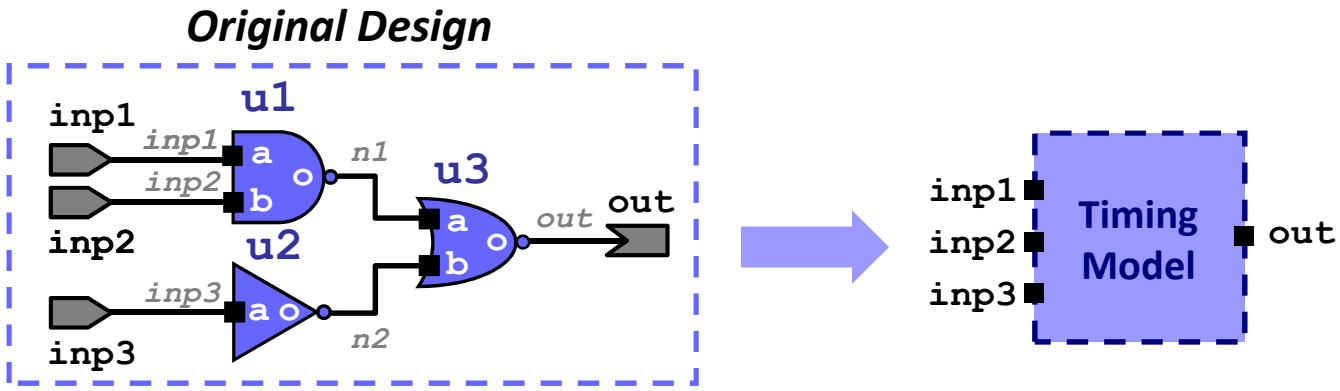
	PATMOS'2011	TAU 2013	TAU 2014	TAU 2015
Delay and Output Slew Calculation	✓	✓		✓
Separate Rise/Fall Transitions	✓	✓		✓
Block / Gate-level Capabilities	✓	✓		✓
Path-level Capabilities (CPPR)†			✓	✓
Statistical / Multi-corner Capabilities		✓		
Incremental Capabilities				✓
Industry-standard Formats (.lib, .v, .spef)				✓

†*CPPR: process of removing inherent but artificial pessimism from timing tests and paths*

Model Size/Performance vs. Accuracy



Timing Model Creation and Usage



Timing Query	Out-of-Context Timing	In-Context Timing
`report_slack -pin inp1`	-15.25	-15.47
`report_slack -pin out`	-20.13	-20.31
`report_slack -pin inp2`	-10.64	-13.91
• • •	• • •	• • •

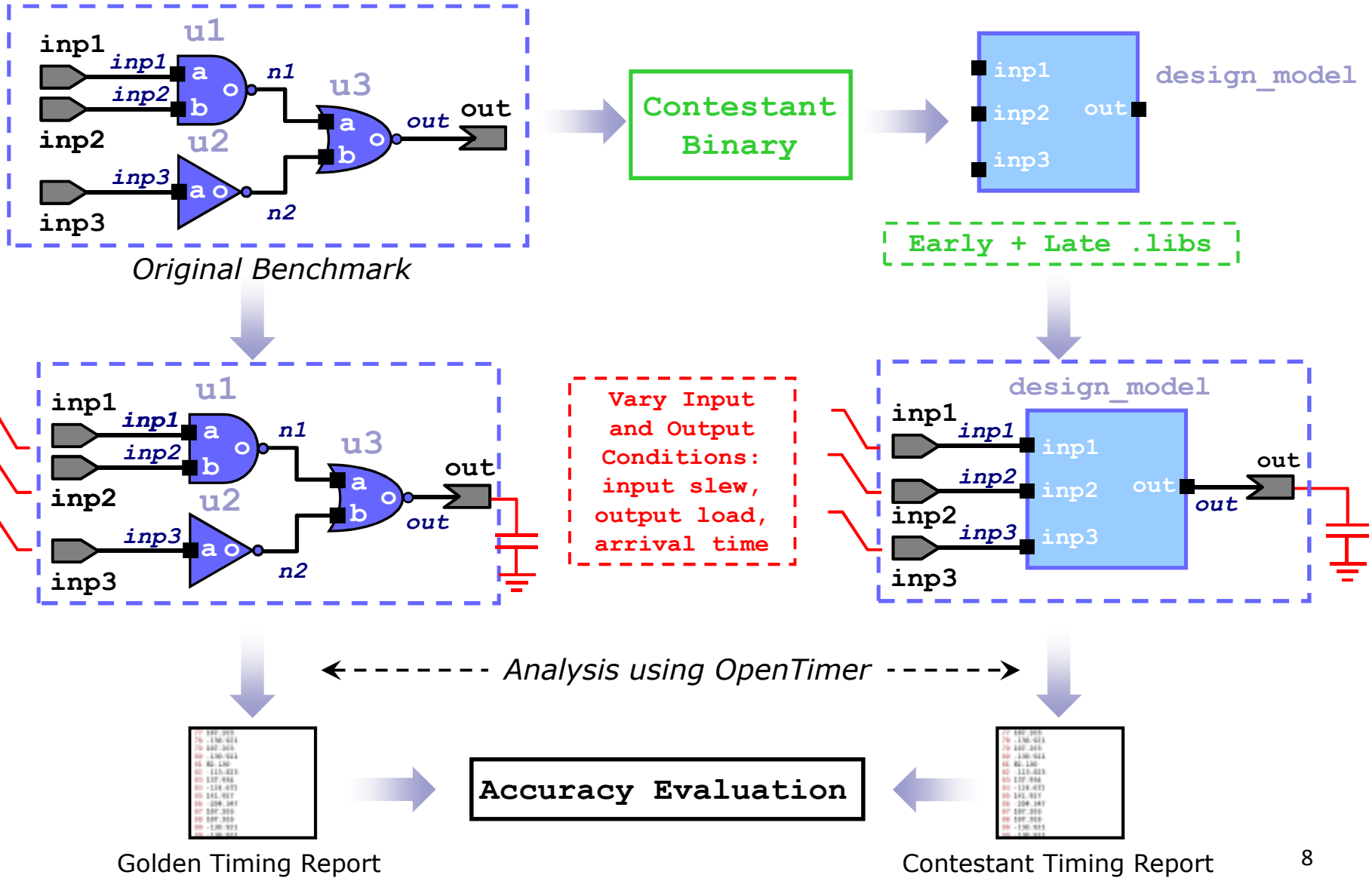
acceptable threshold

Pessimistic, usage dependent

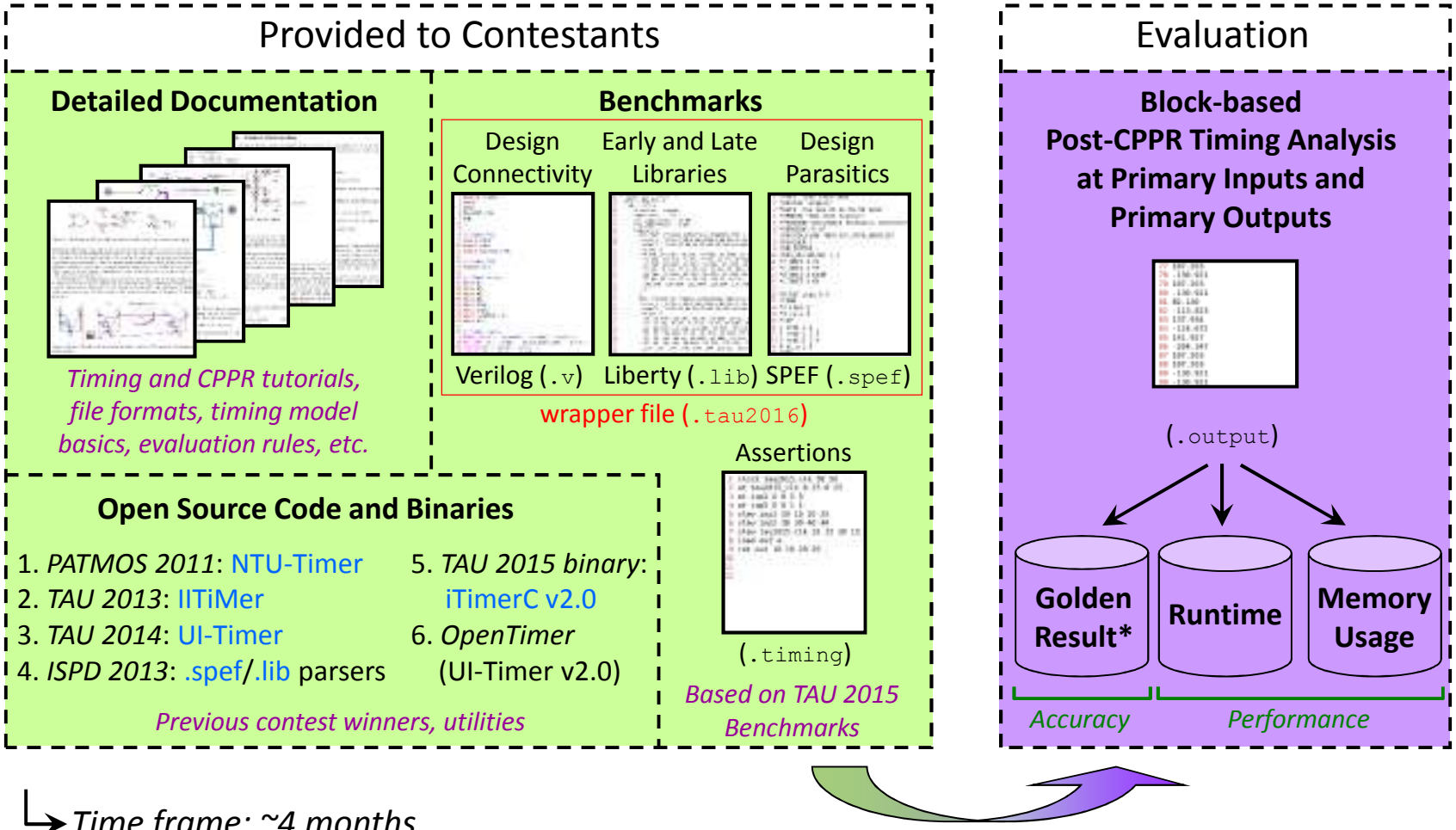
Evaluation based accuracy and performance – both generation and usage

TAU 2016 Contest: target sign-off models (high accuracy),
but strongly consider intermediate usage, e.g., optimization where less accuracy is required

Accuracy Evaluation



TAU 2016 Contest Infrastructure



↳ *Time frame: ~4 months*

↳ *Contest Scope: only hold, setup, RAT tests; no latches (flush segments); single-source clock tree*

**using OpenTimer*

Benchmarks: Binary Development

11 based on TAU 2015 Phase 1 benchmarks (3K – 100K gates)

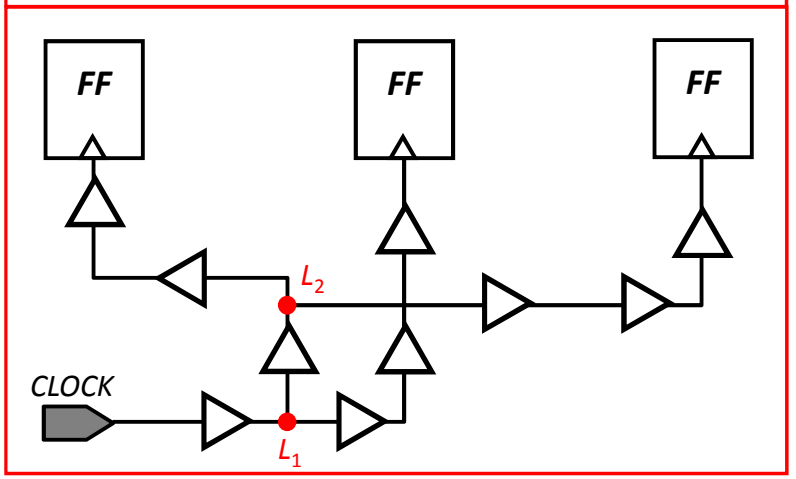
7 based on TAU 2015 Phase 2 benchmarks (1K – 150K gates)

7 based on TAU 2015 Evaluation benchmarks (160K – 1.6M gates)

Design	Number of:			
	PIs	POs	Gates	Nets
ac97_ctrl	84	48	14.3K	14.4K
aes_core	260	129	22.9K	23.2K
des_perf	235	64	105.4K	106.5K
mem_ctrl	115	152	10.5K	10.7K
pci_bridge32	162	207	19.1K	19.3K
systemcaes	260	129	6.5K	6.8K
systemcdes	132	65	3.4K	3.6K
tv80	14	32	5.3K	5.3K
usb_funct	128	121	15.7K	15.9K
vga_lcd	89	109	139.5K	139.6K
wb_dma	217	215	4.2K	4.4K
cordic_ispd	34	64	45.4K	45.4K
des_perf_ispd	234	140	138.9K	139.1K
edit_dist_ispd	2.6K	12	147.6K	150.2K
fft_ispd	1.0K	2.0K	38.2K	39.2K
matrix_mult_ispd	3.2K	1.6K	155.3K	167.2K
pci_bridge_32_ispd	160	201	40.8K	41.0K
usb_phy_ispd	15	19	923	938
b19_iccad	22	25	255.3K	255.3K
mgc_edit_dist_iccad	2.6K	12	161.7K	164.2K
mgc_matrix_mult_iccad	3.2K	1.6K	171.3K	174.5K
vga_lcd_iccad	85	99	259.1K	259.1K
netcard_iccad	1.8K	10	1496.0K	1497.8K
leon2_iccad	615	85	1616.4K	1517.0K
leon3mp_iccad	254	79	1247.7K	1248.0K

Added randomized clock tree [TAU 2014]

- **BRANCH**(*CLOCK*, *initial FF*)
- For each remaining FF
  - Select random location *L* in current tree
  - **BRANCH**(*L*,*FF*)
- **BRANCH** `(src,sink)`: create buffer chain from `src` to `sink`



Benchmarks: Evaluation

10 based on TAU 2015 Phase 1 comb. benchmarks (0.2K – 1.7K gates)

9 based on TAU 2015 Phase 1 seq. benchmarks (0.1K – 1K gates)

6 based on TAU 2015 Phase 2 and Evaluation benchmarks (8.2K – 1.9M gates)

Design	Number of:			
	PIs	POs	Gates	Nets
c432_eval	36	7	0.2K	0.2K
c499_eval	41	32	0.2K	0.2K
c880_eval	60	26	0.3K	0.3K
c1355_eval	41	32	0.2K	0.2K
c1908_eval	33	25	0.3K	0.3K
c2670_eval	157	63	0.5K	0.7K
c3540_eval	50	22	0.9K	0.9K
c5315_eval	178	132	1.3K	1.5K
c6288_eval	32	32	1.7K	1.7K
c7552_eval	206	107	1.5K	1.7K
s27_eval	7	1	<0.1K	<0.1K
s344_eval	11	11	0.2K	0.2K
s349_eval	11	11	0.2K	0.2K
s386_eval	9	7	0.2K	0.2K
s400_eval	5	6	0.3K	0.3K
s510_eval	21	7	0.4K	0.4K
s526_eval	5	6	0.4K	0.4K
s1196_eval	16	14	0.8K	0.8K
s1494_eval	10	19	0.9K	0.9K
tv80_eval	14	32	8.2K	8.2K
mgc_edit_dist_iccad_eval	2.6K	12	222.1K	224.1K
vga_lcd_iccad_eval	85	99	286.4K	286.5K
leon3mp_iccad_eval	254	79	1.5M	1.5M
netcard_iccad_eval	1.8K	10	1.6M	1.6M
leon2_iccad_eval	615	85	1.9M	1.9M

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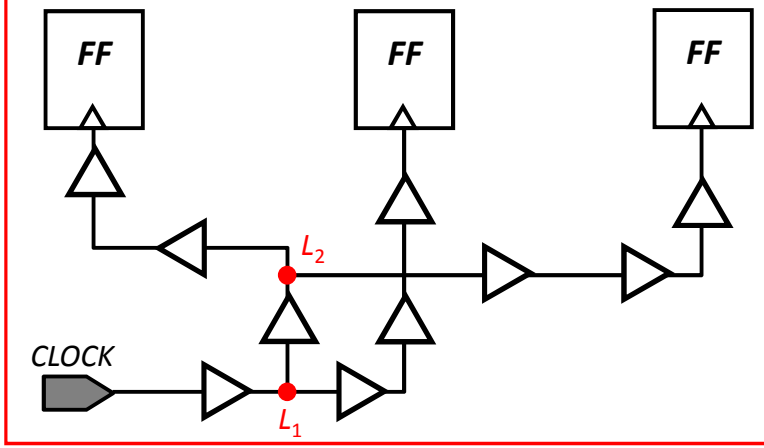
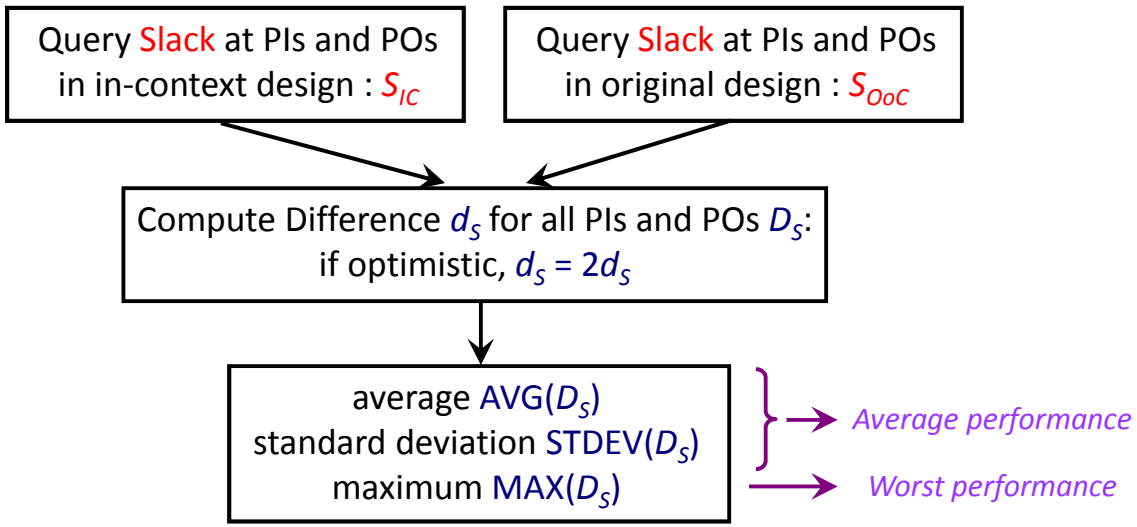


Evaluation Metrics

Accuracy (Compared to Golden Results)



Accuracy Score (Difference)	
[0, 5] ps	100
(5,10] ps	80
(10,15] ps	50
(15,∞) ps	0

Runtime Factor (Relative)

$$RF(D) = \frac{MAX\_R(D) - R(D)}{MAX\_R(D) - MIN\_R(D)} \times R(D)$$

Memory Factor (Relative)

$$MF(D) = \frac{MAX\_M(D) - M(D)}{MAX\_M(D) - MIN\_M(D)} \times M(D)$$

Composite Design Score

$$score(D) = A(D) \times (70 + 20 \times RF(D) + 10 \times MF(D))$$

Overall Contestant Score is average over all design scores

TAU 2016 Contestants

	University	Team Name
	Drexel University	Dragon
	University of Illinois at Urbana-Champaign	LibAbs
	University of Minnesota, Twin Cities	--
	University of Thessaly	too_fast_too_accurate
	India Institute of Technology, Madras	Darth Consilius
	India Institute of Technology, Madras	IITMTimers
	National Chiao Tung University	iTimerM

Contestant Results: Accuracy

Top 2 Teams: Very different generated models

- 25 designs: Both teams have high accuracy on 21 of them (< 1 ps max difference)
- Team 1: very consistent on high accuracy

Benchmark	Team 1	Team 2
mgc_edit_dist_eval	0.31	0.51
vga_lcd_iccad_eval	0.43	0.83
leon3_iccad_eval	0.42	30.7
netcard_iccad_eval	0.19	90.9
leon2_iccad_eval	0.24	126.5
Accuracy Average (all)	**1.00**	**0.94**

Contestant Results: Runtime (s)

Top 2 Teams: Very different generated models

- Team 1 has better generation time
- Team 2 has better in-context usage runtime (preferred)

		Generation		Usage	
Benchmark	Original	Team 1	Team 2	Team 1	Team 2
`mgc_edit_dist_eval`	8	64	112	19	20
`vga_lcd_iccad_eval`	10	79	107	24	16
`leon3_iccad_eval`	64	437	364	143	1
`netcard_iccad_eval`	69	473	996	148	67
`leon2_iccad_eval`	77	552	1125	182	144
Runtime Average (all)	1x	**7x**	**12x**	**2x**	**1.05x**

Contestant Results: Memory (GB)

Top 2 Teams: Very different generated models

- Team 1 better memory for larger benchmarks; Team 2 better for smaller
- Team 1 and 2 relatively same memory during in-context usage

		Generation		Usage	
Benchmark	Original	Team 1	Team 2	Team 1	Team 2
mgc_edit_dist_eval	1.9	2.7	4.5	3.7	5
vga_lcd_iccad_eval	2.35	3.3	5	4.3	4
leon3_iccad_eval	11	16.7	18.6	23.1	0.6
netcard_iccad_eval	12.7	18.6	29.4	23.6	16
leon2_iccad_eval	14.2	22	36.3	30.1	34.4
Memory Average (all)	1x	**1.2x**	**0.5x**	**0.85x**	**0.8x**

Contestant Results: Model Size

not considered during evaluation

Top 2 Teams: Very different generated models

- Team 1: better accuracy, fast generation runtime
- Team 2: faster usage runtime, better generation memory

Needs accuracy fix

	Gates + Nets (estimate)	Timing Arcs		Internal Pins	
Benchmark	Original	Team 1	Team 2	Team 1	Team 2
mgc_edit_dist_eval	446K	400K	178K	300K	62K
vga_lcd_iccad_eval	570K	500K	150K	350K	51K
leon3_iccad_eval	3M	3M	8K	2M	3K
netcard_iccad_eval	3.2M	3.1M	675K	2M	267K
leon2_iccad_eval	3.8M	3.8M	1.3M	2M	430K
Model Size Average (all)	1x	**1.27x**	**0.72x**		
Model Size Average (seq)	1x	**1.08x**	**0.35x**		

Contest places highest emphasis on accuracy (target sign-off timing)

Acknowledgments

Song Chen
Contest Committee Member

Xin Zhao
Contest Committee Member

Xi Chen
Contest Committee Member

Debjit Sinha
Workshop General Chair

Qiuyang Wu
Workshop Technical Chair

Tsung-Wei Huang
OpenTimer Support

The TAU 2016 Contestants

*This contest would not have been successful without your **hard work** and **dedication***

TAU 2016

Timing Contest on Macro Modeling

Honorable Mention

Presented to

Pei-Yu Lee, Ting-You Yang, Wei-Chun Chang, Ya-Chu Chang, and Iris Hui-Ru Jiang

For

iTimerM

National Chiao Tung University, Taiwan

Debjit Sinha	*Qiuyang Wu*	*Jin Hu*
General Chair	Technical Chair	Contest Chair

TAU 2016

Timing Contest on Macro Modeling

Contest Winner

Presented to

Tin-Yin Lai, Tsung-Wei Huang, and Martin D. F. Wong

For

LibAbs

University of Illinois at Urbana-Champaign, USA

Debjit Sinha	*Qiuyang Wu*	*Jin Hu*
General Chair	Technical Chair	Contest Chair

Looking Forward to 2017 and Beyond

Macro Modeling Reflections

- Accuracy results are very impressive!
- Learning experience for both contestants and organizers for Round 2:
  - Focus on different evaluation metrics (e.g., less emphasis on accuracy)
  - Consider more constraints (e.g., performance) while maintaining accuracy
  - Better understanding about different implementations and approaches
- Further study tradeoffs between accuracy and performance
  - LibAbs and iTimerM and industry approaches significantly different
  - Different evaluation "grades" (potentially vs. industry results)

TAU 2017 Contest Plans

- Different timeline to overlap with a semester or quarter
- More coordination with universities (e.g., integrate into coursework)
- More realistic feedback process for debugging / improving tools

If you have ideas, come talk to us!

tau.contest@gmail.com

Backup