DISCUSSION PANEL

AGING EFFECTS MODELING AND ANALYSIS

MODERATOR: CHRISTIAN LUTKEMEYER, INPHI CORP.
AGING
PANELISTS

• Andrew Kahng, UCSD
• Mehmet Avci, Intel
• Debjit Sinha, IBM
• Patrick Groeneveld
• Igor Keller, Cadence
• Paul Penzes, Qualcomm
THE CONSUMER VIEW ON DEVICE AGING

• After working well for a few years my WIFI router needed to be power-cycled more and more often ...

• Out of warranty => get a new device => more features, higher bandwidth
LIFE EXPECTANCY GUIDELINES

<table>
<thead>
<tr>
<th>INDUSTRY GROUP</th>
<th>ASSET RANGE</th>
<th>LIFE IN YEARS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sugar and sugar products manufacturing</td>
<td>14.5</td>
<td>18</td>
</tr>
<tr>
<td>Telephone, central office equipment</td>
<td>28</td>
<td>35</td>
</tr>
<tr>
<td>distribution</td>
<td>8</td>
<td>10</td>
</tr>
<tr>
<td>station equipment</td>
<td>7</td>
<td>9</td>
</tr>
<tr>
<td>Textile products, including finishing and dyeing</td>
<td>7</td>
<td>9</td>
</tr>
</tbody>
</table>

| Brewery equipment                                        | 9.5         | 12            |
| Cable television, headend facilities                     | 9           | 11            |
| microwave systems                                        | 7.5         | 9.5           |
| program origination                                     | 7           | 9             |
| service and test                                         | 7           | 8.5           |
| subscriber connection and distribution                   | 8           | 10            |
| Canneries and frozen food production                     | 9.5         | 12            |

Source: MARSHALL VALUATION SERVICE

Submarine fiber optic cables with repeaters every 80km-100km: 25 years!
ANDREW B. KAHNG

• is Professor of Computer Science and Engineering, and Electrical and Computer Engineering at UC San Diego. He has been a visiting scientist at Cadence (1995-1997) and founder/CTO at Blaze DFM (2004-2006). His research interests include IC physical design and performance analysis, the IC design-manufacturing interface, combinatorial algorithms and optimization, and the roadmapping of systems and technology.

• 400 journal and conference papers, 3 books, 33 issued patents; fellow ACM and IEEE, chaired DAC, ISQED, ISPD and other conferences.
**FEOL Aging Taxonomy**

A. Dielectric wear-out/breakdown (TDDB)
   - Due to broken Si-O bonds

B. Threshold voltage instability
   - BTI
   - HCl
   - Due to broken Si-H bonds

**Scaling/Device Challenges**

**Fin Geometry**
- Fin profile
- Sidewall surface orientation
- Self-heating

**Pitch scaling**
- Gate and S/D spacing < 10nm
  - Sidewall spacer reliability

**Statistical Modeling**
- Device contains only handful of defects
  - Statistical degradation
    - Reliability
    - Increased performance
    - Variability
    - Uncertainty

- Characterization, modeling and analysis, signoff (STA) criteria, synthesis/optimization...
NEGATIVE BIAS TEMPERATURE INSTABILITY (NBTI)

- Stress + Recovery (‘healing’)
- Power-law (front-loaded)
- Exponential w/temperature
- Strong voltage dependency

- **Design:** temp, guardbands/libs, adaptivity (AVS), gating, race-to-halt ...

@N10, N7: NBTI vs. PBTI (PMOS-dominated paths, FFs); worse self-heating
BTI AGING LIB CHARACTERIZATION, SIGNOFF WITH AVS

- $V_{BTI}$: used to characterize BTI degradation, i.e., amount of $\Delta V_T$ shift
- $V_{lib}$: used to characterize standard cells

AVS-aware aging signoff – issues

- Guardbands: $V_{BTI}$ worst case is high; $V_{lib}$ worst case is low
- Chicken-Egg: $V_{FINAL}$ depends on implementation

Aging and $V_{FINAL}$ are not known before circuit is implemented

**Diagram:**
- Step 1: $V_{BTI}$, $|\Delta V_T|$, $V_{FINAL}$
- Step 2: Derated library, BTI degradation and AVS
- Step 3: Circuit implementation and signoff

?
AGING-, AVS-AWARE SIGNOFF CORNER SELECTION

- Case 1: $V_{DD} = V_{init}$ → Ignore AVS
- Case 2: Worst case scenario in derated library
- Case 3: $V_{DD} = V_{max}$ → extreme case for AVS
- Case 4: $V_{bti} = V_{final}$ → does not overestimate aging but ignore AVS
- Case 5: No derated library (reference)
- Case 6: (UCSD, DATE-2013 paper) → can do simple things before “boiling the ocean”

![Graph showing signoff corner selection with optimistic and pessimistic corners.](image-url)
HOT CARRIER INJECTION

- Channel carriers driven toward gate oxide before reaching drain when $V_G \sim V_D$
  - I.e., when device “turns on hard”

- Worst case: high switching activity, large input slew, large output load

- Few such devices in SOC (N.B.: max trans, max cap DRCs don’t help too much!)

- Design: control slews, activity factors, loads (= not a surprise);
  NAND-based logic design (?)…
TIME DEPENDENT DIELECTRIC BREAKDOWN (TDDB)

Damage to dielectric (1) at gate oxide or (2) between metal lines

- Oxide defects accumulate over time
- As more traps are created, overlapping defects form conductive path → soft breakdown
- Conduction → heat → thermal damage → more defects → more conduction
- Oxide melts in the breakdown spots → conductive filament forms → hard breakdown
GATE OXIDE BREAKDOWN (TDDB), SRAM

- TDDB = soft breakdown, is self-limited
  - N2 aging $\rightarrow$ stress-induced leakage $I_{\text{gate}}$ increase
  - $\rightarrow$ on-resistance of P1 reduces gate voltage and stress on N2
  - Standby current increases

- SRAM: degrades read and write margins, and $V_{\text{cc}_{\text{min}}}$

$\rightarrow$ Hence: **TDDB limits $V_{\text{max}}$ of SRAM**

- Design: add $f_{\text{max}}$ margin, use larger bitcells, flip bits (wear-leveling), reduce $V_{\text{DD}}-V_{\text{SS}}$ during standby, ECC, ...
“STATE OF PLAY” (@TAU)

• Not much change since DAC-2013 Reliability Panel (!)
  • Acknowledgments / Thanks: Martin St. Laurent, Kee Sup Kim

• Presilicon aging analysis: no major challenges
  • But, what do you feed it (e.g., probability distributions of signals)?
  • And, how will you use this? (Will you end up with a different tapeout? See any “signal”?)
  • (N.B.: Industry will always defer or work around added model complexity …)
  • (What’s okay for EM, DVD signoff = okay for aging signoff?)

• Closing the gap between worst-case design and in-the-field reality…
  • Monitoring and feedback = long-standing idea
  • Standard IPs and EDA support needed (what about “learning”?)

• …Competes with improvements in design methodology (e.g., signoff criteria!) and synthesis, optimization tools (e.g., path PMOS-dominance)
  • Understand implications of adaptivity! + Tie-ins for analysis, analysis macromodels

• Memories, power specs may provide some kind of forcing function …
MEHMET AVCI

- Mehmet Avci received the B.S. degree in electrical and electronics engineering from the Middle East Technical University and the M.A.Sc. degree in electrical and computer engineering from the University of Toronto. He is currently working at the Intel Toronto Technology Centre in Toronto, ON, Canada as a Design Engineer focusing on timing modeling and analysis.

His research interests include computer-aided design (CAD) for integrated circuits, with a focus on timing modeling and analysis, as well as power modeling and grid analysis.
Intel PSG Aging Modeling

Mehmet Avci
Intel PSG Aging Modeling

- Aging modeling includes both BTI and HCI.
- Base models are BOL (Beginning-of-Life).
- These BOL models are then scaled by a factor (i.e. aging factor) which includes both BTI and HCI effects.
- This factor covers the possible worst-case aging under any scenario.
  - Calculated via simulation.
  - Correlated with silicon measurements.
- This worst-case factor would have non-negligible Fmax loss if we can’t reclaim some of this pessimism.
  - Inter-clock transfers would be impacted more due to lack of CCPR.
Aging Pessimism Removal – Same Clock Domain

- Common portion pessimism will be reclaimed by CCPR
- Separate clock path portion would see the full worst-case aging
- Green Clock Segment will be covered by CCPR
- Purple segments have:
  - Same duty-cycle
  - Same static probability
- Aging contribution to the pessimism can be removed
Aging Pessimism Removal – Gated Clocks and Between Related Clocks

- Gated clocks: aging pessimism removal depends on the location of the gate
- Related Clocks: aging pessimism can be removed assuming if the clocks have same duty-cycle and frequency difference between clocks is not huge

DEBJIT SINHA

is a Senior Engineer/Scientist in IBM EDA. He joined IBM after a PhD in EECS from Northwestern University. At IBM, he has lead several teams including noise analysis, statistical timing for IBM servers, and timing macro-modeling. Debjit is the author of 40+ papers and a co-inventor for 20+ patents. He organized the first TAU timing contest in 2013, and has been actively involved in TAU since!
TAU 2017 panel: Aging effects and modeling

Debjit Sinha
IBM Electronic Design Automation
IBM Systems, Poughkeepsie, NY

March 16-17, 2017
TAU 2017 – Monterey, CA
Aging effects and modeling

- Contributors modeled
  - Hot carrier injection (HCI) [also termed Hot electron]
  - [Negative-/Positive-] bias temperature instability (NBTI/PBTI)
  - Electromigration (EM)
  - ...

- Modeling (outside scope of EDA/timing) – Multiple stages
  - Simulation based – Using IBM PowerSpice/PowerRel, Cadence Spectre/RelXpert
    - Representative gates, circuits
    - Different stress modes – Uni-/Bi-polar, DC
  - Capture impact in device model, functional simulation
    - Representative circuits, critical design components (memory, clocking elements – buffers, latches)
  - Hardware testing
    - Burn in (BI), High temperature operating life (HTOL), End of life (EOL)
    - Model to hardware correlation for next design iteration
Modeling aging effects in timing [analysis/optimization] tools

- **IBM ASICs (32nm and older)**
  - Standard cell timing model – Function of PVT, …, and aging
  - Statistical timing analysis with parameter – ProductReliability
    [k sigma range for BeginningOfLife (BOL) : EndOfLife (EOL)]
    • Non-linearities handled

- **IBM Servers**
  - Margining approach
    • Clock period guard-band
    • Critical path simulation based validation for cycle time independent tests
    • Capacitance [max. load] limits in standard cells for signal EM (SEM), current/dimension rules for wires
    • Power grid analysis models EM for power network
  - Simulation based for SEM in transistor level timing
    • Can compute current during simulation, test against EM rules
  - Robust corner analysis via simulations
    • E.g.: Critical circuit components – Strong/weak PFET/NET with BOL/EOL
Sophisticated aging modeling in timing – Needed?

- High level – Balanced clock and data paths aging similarly?
  - Detail level – Non-uniform, difficult to model accurately

- Aging not just a function of power on hours (POH)
  - Function (switching activity) dependent
    - E.g.: Rare switching in error detection circuits

- Cell EM analysis during timing
  - More challenging to model than wire EM

- Final impact and margin
  - Design for robustness – Stacked devices in latches*
  - Single digit % margin
  - Worth additional investment at this point – Perhaps not!
    [Given constrained resources]
Patrick Groeneveld was Chief Technologist at Magma Design Automation since its inception. He designed the revolutionary RTL to GDS2 flow which is based on a unique common data model. It combined a native sign-off STA tool that drives various logical and physical synthesis tools. After acquisition by Synopsys he worked on optimization in Design Compiler. Patrick was chair of DAC and was full professor in EE at Eindhoven University. He holds a Ph.D. in EE from Delft University of Technology.
AGING: A SYNTHESIS FLOW PERSPECTIVE

• What is the core problem?
  • Aging increases $V_t$ because carriers enter the oxide, slowing down gates over time.
  • Electromigration causes failure in wires.

• Can we design for aging?
  • Yes, but there is no free lunch: area and dynamic power will suffer.

• How to design for aging?
  • Just add another corner to add pessimism for aging.

• Can we do more during design?
  • Not much. Since activity data is unknown, looking at regeneration and duty cycle make little sense. We need to ‘suck up’ aging effects just like other sources of variability.
IGOR KELLER

• is a Distinguished Engineer at Cadence Designs Systems. During his 15-years tenure at Cadence he has been working on signal integrity, delay calculation, variability and reliability in timing as part of the analysis infrastructure used in P&R and signoff products. Prior to Cadence he worked at Intel developing in-house static noise and timing analysis solutions. Igor received his Master and PhD degree in Mechanics and Applied Mathematics from University of Perm, Russia. He holds more than 30 patents in delay calculation and related areas and is active in conferences and workshops, including TAU.
AGING MODELING

• Multiple factors involved
  • Calendar Age, Temperature, Vdd, Duty Cycle, Switching Activity, on/off ratio

• Multiple underlying physical phenomena
  • HCI
    • Switching Activity
  • BTI
    • Duty cycle, recovery

• Inherently vector dependent

• Need aging model for devices
  • Not easy to extract from silicon
BUSINESS VIEW

• Business segments narrow: Automotive, high-end communication
  • Market is small but growing fast
  • Still not a commodity

• Significant investments needed
  • ROI not clear
  • Requires expertise in device physics
  • Joint research and data sharing with foundries

• Use models different between digital, analog, mixed-signal

• Good news: we know how to do it
  • If there is a will, there is a way
AGING IN STA: CHALLENGES AND IDEAS

• Aging device model: no standard, not comprehensive, costly
  • Statistical model breaks down for small devices at low geometries

• Cell Model/Library:
  • High dimensionality, spanning all parameters on top of PVT isn’t practical
  • Need a concept of Effective Age: the only new parameter
    • Not clear if \{Calendar Age, DC, SA, on/off ratio\} can be converged into 1D EA

• STA:
  • Increase in number of scenarios
  • SA, DC are hard to compute, need vectors
  • Each instance ages differently
    • Clocks is major concern: high activity, rise/fall, launch/capture skew
PAUL PENZES

• is a Senior Director of Engineering at Qualcomm Technologies Inc. He leads the Design Technology (DTECH) team within the Central Engineering and Technology organization. He manages design technology integration, digital testchips, timing methodology and sign-off, and performance-power-area (PPA) R&D. Prior to Qualcomm, Paul was an Associate Technical Director and Distinguished Engineer at Broadcom Inc. Paul has +25 patents issued, +15 pending, and has a B.S., an M.S. and a Ph.D. in Computer Science from the California Institute of Technology, Pasadena.
PANEL DISCUSSION, QUESTIONS AND ANSWERS