



TAU 2017 Program

<http://www.tauworkshop.com>

March 16-17, 2017

Monterey Marriott, Monterey, California, USA

Thursday, March 16, 2017

8 – 9:00 a.m. Breakfast

9:00 – 9:15 a.m. Opening Remarks from general chair

9:15 – 10:00 a.m. Recent Advances in Timing Analysis [Keynote] (Chair: Qiuyang Wu, Synopsys)

Speaker: Martin Wong (ECE, University of Illinois Urbana-Champaign)

10:00 – 10:15 a.m. Break

10:15 – 11:15 a.m. Interconnect Modeling and Optimization (Chair: Subramanyam Sripada, Synopsys)

1. *A Scaling-based Approach for Fast Multiple PVT Corner Analysis with Guaranteed Circuit Timing*
Mehmet Avci (Intel)
2. *Using RICE for FPGA Routing Delay Annotation*
Andrew Clinton (Intel)
3. *Multiple Personality Disorder of Cell Models - A Cure By Transistor*
Shiva Raja, Joao Geada, Qian Shen and Nick Rethman (CLK-DA)

11:15 – 12:00 p.m. Adventures the Candy Land of Timing Modeling (Chair: Qiuyang Wu - Synopsys)

Speaker: Bogdan Tutuianu (TSMC)

12:00 – 2:00 p.m. Lunch and social networking

2:00 – 2:45 a.m. Are You Ready to Re-Time Your Design? [Keynote] (Chair: Joao Geada, CLK-DA)

Speaker: Mahesh Iyer (Intel, Programmable Solutions Group)

2:45 – 4:05 p.m. Design Optimization (Chair: Tom Spyrou, Intel)

1. *An Exact Polynomial Time Algorithm for Clock Tree Sizing for Register Files*
Alexander Berkovich, Lawrence Gonzales, Rupesh Shelar and Ataur Patwary (Intel)
2. *Reduction of Compute Resources for Signoff-driven ECO*
Nahmsuk Oh, Subramanyam Sripada and Qiuyang Wu (Synopsys)
3. *Efficient Incremental Flow for signoff-driven ECO*
Subramanyam Sripada and Song Chen (Synopsys)
4. *Variable Bandwidth Links for Self-Timed On-Chip Communication*
Shomit Das and Greg Sadowski (AMD)

4:05 – 4:30 p.m. Break

4:30 – 6:00 p.m. Panel: Aging Effects Modeling and Analysis

Organizer: Christian Lutkemeyer (inPhi)

Panelists: Andrew Kahng (UCSD), Kazutoshi Kobayashi (KIT, Japan), Igor Keller (Cadence), Bogdan Tutuianu (TSMC), Paul Penzes (Qualcomm)

7 – 9 p.m. Reception

Friday, March 11, 2016

8 – 9:00 a.m. Breakfast

9:00 – 9:15 a.m. Opening Remarks from technical program chair

9:15 – 10:00 a.m. Timing and Power Analysis (Chair: Tom Spyrou, Intel)

Speaker: Bill Mullen (Ansys)

10:00 – 10:45 a.m. Rogue Waves, On-Chip Power Integrity, and Static Timing Analysis (Chair: Jindrich Zejda, Xilinx)

Presenters: Christian Lutkemeyer (inPhi)

10:45 – 11:00 a.m. Break

11:00 – 11:45 a.m. TAU contest: Timing macro-modeling (Chair: Tom Spyrou, Intel)

Presenters: Song Chen (Synopsys)

11:45 – 12:15 p.m. A New SSTA Method Based On Birnbaum-Saunders Distribution [Invited Talk]
(Chair: Song Chen)

Speaker: Mikhail Chetin and Praveen Ghanta (Cadence Design Systems)

12:15 – 2 p.m. Lunch and social networking

2:00 p.m. – 3:00 p.m. Design Reliability (Chair: Oscar Ou, MediaTek)

1. *Circuit Analysis and Defect Characteristics Estimation Methods Using Bimodal Defect-Centric Random Telegraph Noise Model*

Michitarou Yabuuchi, Azusa Oshima, Takuya Komawaki, Ryo Kishida, Jun Furuta, Kazutoshi Kobayashi, Pieter Weckx, Ben Kaczer, Takashi Matsumoto and Hidetoshi Onodera (Kyoto Institute of Technology)

2. *Parametric Timing Yield Aware Design considering Random Variation Impact*

Moon Su Kim (Samsung)

3. *Practical Statistical Static Timing Analysis with Low Cost Statistical Library and Residual Sigma Propagation*

Jongyoon Jung (Samsung)

3:00 – 4:30 p.m. Panel: Power, Rail and Timing Analysis

Organizer: Igor Keller (Cadence)

Panelists: Christian Lutkemeyer -Clariphy, Bill Mullen – Ansys, Jim Dodrill, ARM, Paul Penzes - Qualcomm, Harish Kriplani – Synopsys

*Invited papers/abstracts

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