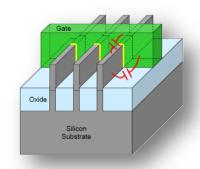
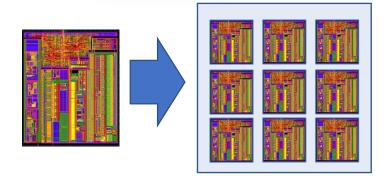
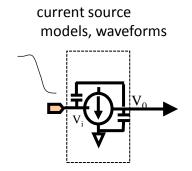


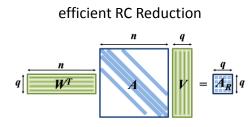
Motivation

- Design trends:
 - Finfet era: faster cells, higher logic density, clocks scale down fast
 - Size grew significantly: 109-instance designs are here!
 - Higher process variations: many process corners, often >100
- Requirements for modern STA:
 - High capacity and performance
 - Required accuracy: path delay within 2% of Spice
 - Waveform Aware Simulation-based delay calculation is a MUST







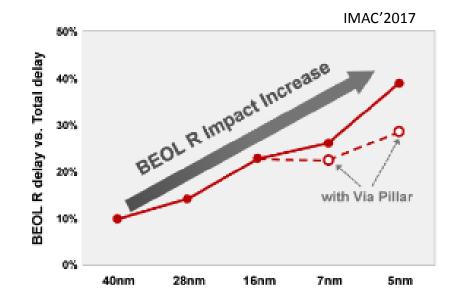


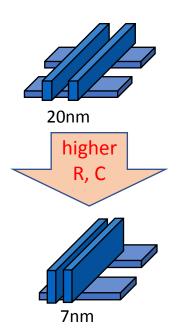
Fast and accurate ODE solvers

$$E\dot{x} = Ax + BI(t, v, \tau)$$
$$v = Cx$$

Motivation, cont.

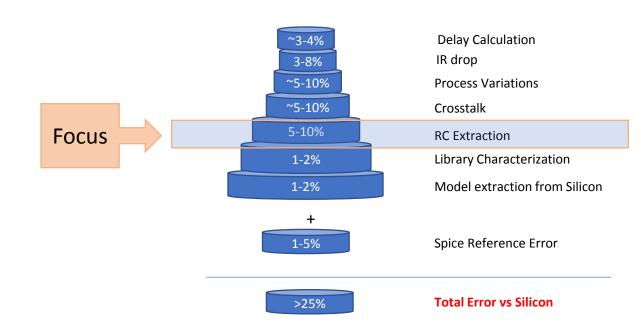
- Shrinking geometries lead to higher resistance and capacitance of wires
 - Good old times of C_{eff}+TLU delay calculation are over!
- Wire delays scale down slower than cell delays





Motivation, cont.

- Many sources of inaccuracy in STA
- Is Spice an ultimate reference for delay?
 - Not really, uses many assumptions
- Wire has a continuous though non-uniform resistance and capacitance
- RC extraction replaces it with lumped R's and C's
 - Lumping: *spatial discretization*
- Effects of spatial discretization on STA accuracy is not well studied
 - Goal of this work

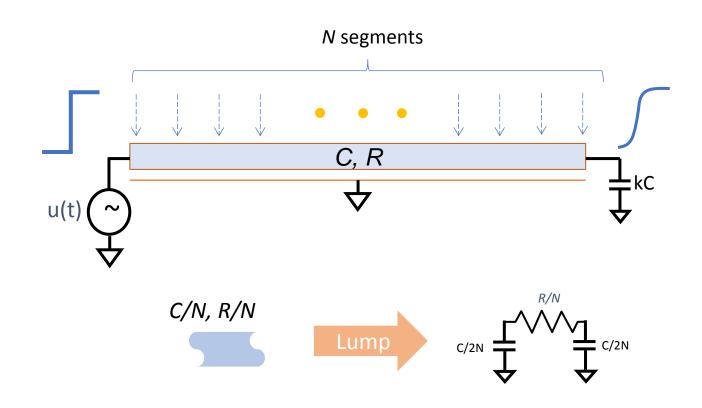


RC Extraction => Spatial discretization



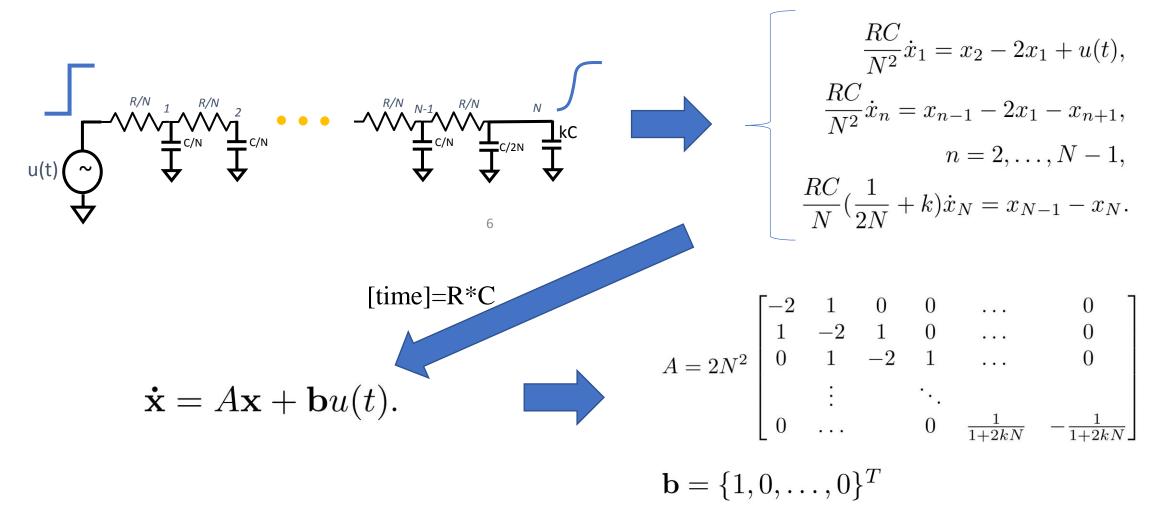
Problem Formulation

- Uniform wire, far-end cap
 - Driver: step voltage source
 - Target: far-end voltage response
- Split into N equal segments
- Approximate each with Π -model
- Build N-link RC chain
- Goal: accuracy of far-end response vs N



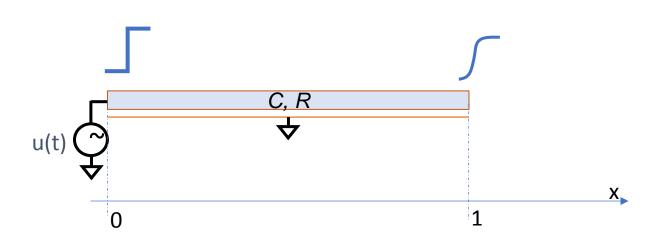


Discretized Problem, Numerical Solution



6

Continuous Problem, Analytical Solution

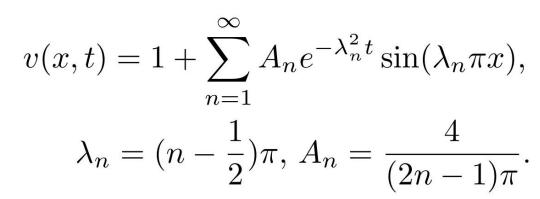


[time]=R*C

t=0:
$$v(0,x) = 0,$$
boundary conditions at x=1: $\frac{\partial v}{\partial x} = k \frac{\partial v}{\partial t},$

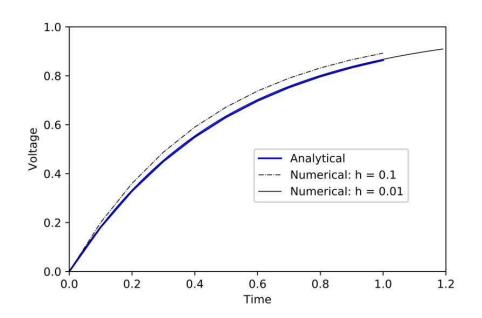
$$v(t,0) = u(t).$$

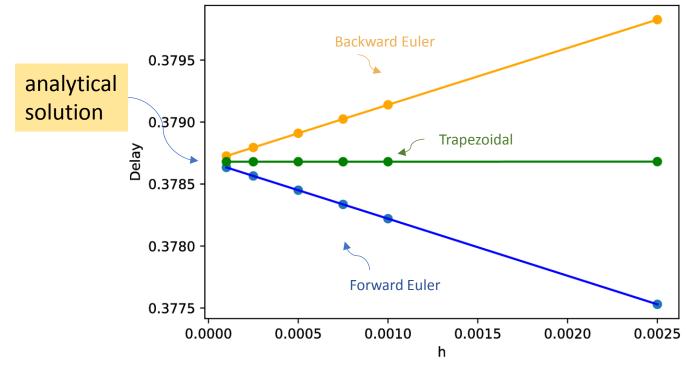
Solution:



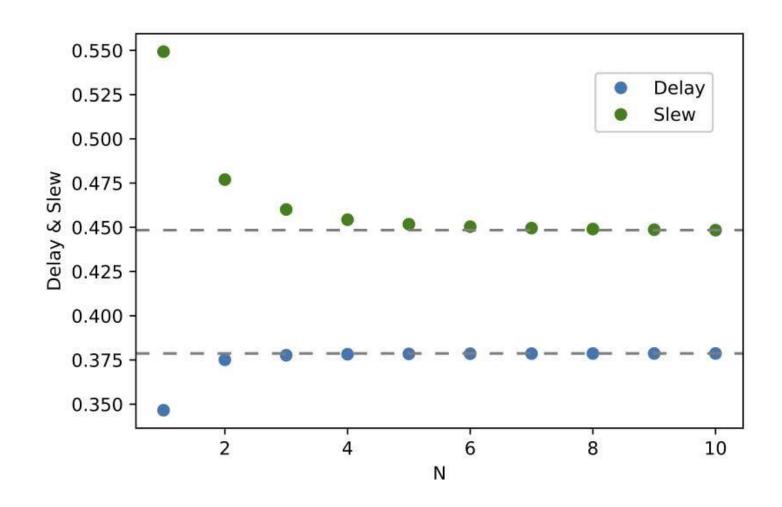
Errors of Temporal Discretization

- Numerical solution of ODEs has errors due to temporal discretization
- Needs to be much smaller than spatial discretization
- Errors depends on the method
 - Backward/Forward Euler: O(h)
 - Trapezoidal: $O(h^2)$

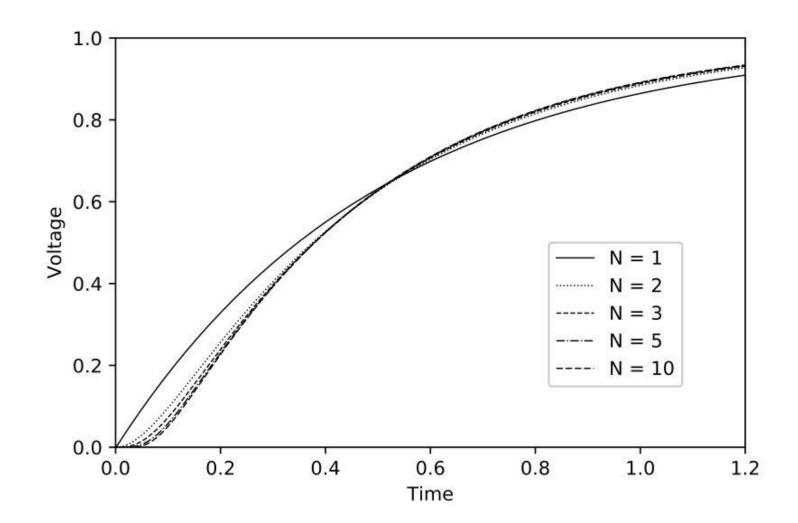




Accuracy of Wire Delay and Slew (k=0)



Voltage Responses at Far End



Results

Delay, slew and relative errors for different far-end load and N

Time unit = R*C

	Slew			Delay			Slew Error (%)			Delay Error (%)		
N	k = 0	k = 1	k = 2	k = 0	k = 1	k=2	k = 0	k = 1	k = 2	k = 0	k=1	k = 2
1	0.549	0.549	0.549	0.347	0.347	0.347	22.51	-63.04	-78.68	-8.479	-68.15	-80.56
2	0.477	1.526	2.617	0.375	1.079	1.772	6.374	2.659	1.590	-0.945	-0.835	-0.587
3	0.460	1.503	2.593	0.378	1.085	1.778	2.603	1.109	0.668	-0.269	-0.334	-0.241
4	0.454	1.495	2.585	0.378	1.086	1.780	1.320	0.574	0.346	-0.119	-0.170	-0.123
5	0.452	1.491	2.581	0.378	1.087	1.781	0.745	0.327	0.198	-0.063	-0.096	-0.070
6	0.450	1.489	2.579	0.379	1.088	1.782	0.439	0.194	0.117	-0.034	-0.057	-0.042
7	0.450	1.488	2.578	0.379	1.088	1.782	0.254	0.114	0.069	-0.021	-0.033	-0.024
8	.449	1.487	2.577	0.379	1.088	1.782	0.136	0.061	0.037	-0.011	-0.018	-0.013
9	0.449	1.487	2.576	0.379	1.088	1.783	0.056	0.026	0.016	-0.005	-0.008	-0.006
10	0.448	1.486	2.576	0.379	1.088	1.783	0.0	0.0	0.0	0.0	0.0	0.0

Conclusions, Future Work

- Spatial discretization in RC extraction may cause large errors
- We quantified errors of wire delay and slew for several far-end loads
- Used analytical solution to ensure time discretization has negligible error
- We demonstrated that number of segments needs to be larger than 2 for wire delay error < 2%
 - Is important for wire-delay dominated paths
- Future work:
 - include crosstalk
 - more complex wire topologies
 - non-uniform wire widths and spacing