A GRAPH BASED APPROACH FOR COMPUTATION REDUCTION FOR MULTI INPUT SWITCHING

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Agenda

1. Introduction

2. Challenges in MIS modelling

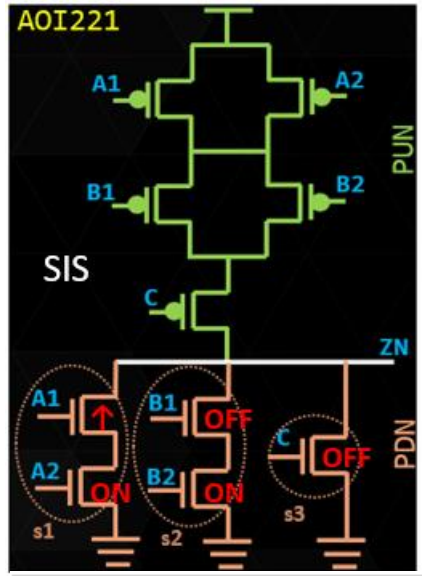
3. Pattern Reduction Algorithm for MIS

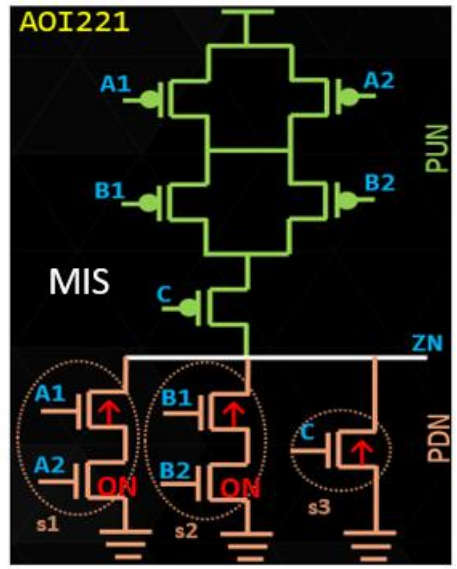
4. Results

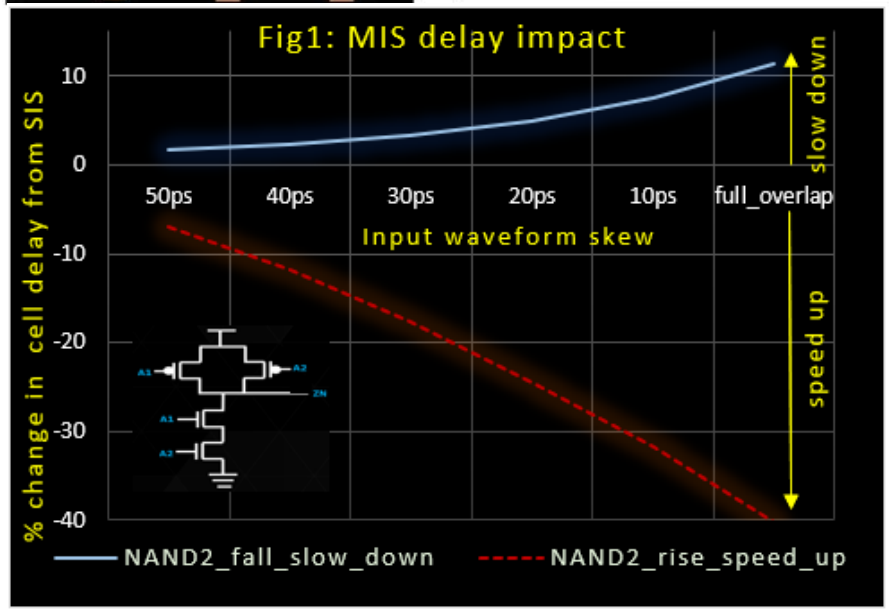
5. Comparison with an industry STA tool MIS solution

Multi-Input Switching

- In STA, delay from A1 to ZN is SIS modelling. Other inputs at their non-controlling values.
- MIS causes both speed-up and slow-down. Impacts Delay, Output Trans
- Speed-up effects are more, hence hold impacting.
- EDA tool handle has Lib cell based MIS coefficient multiplied with SIS cell delays during delay calculation when MIS is enabled.
- Advanced MIS in EDA tools looks better but not fully encapsulating MIS.





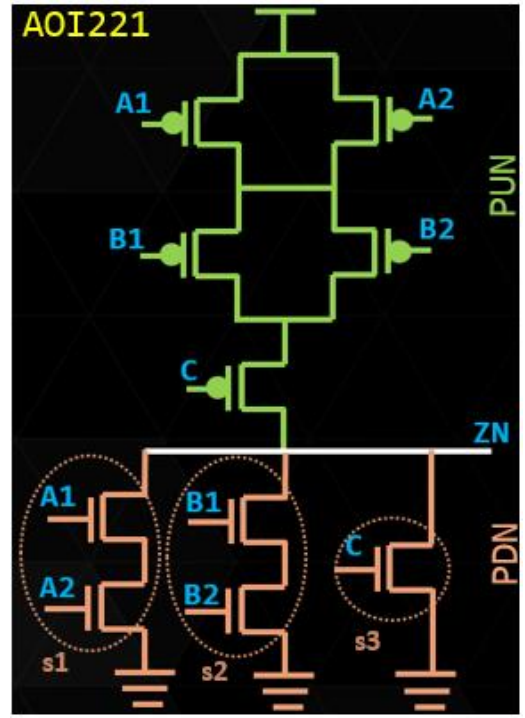


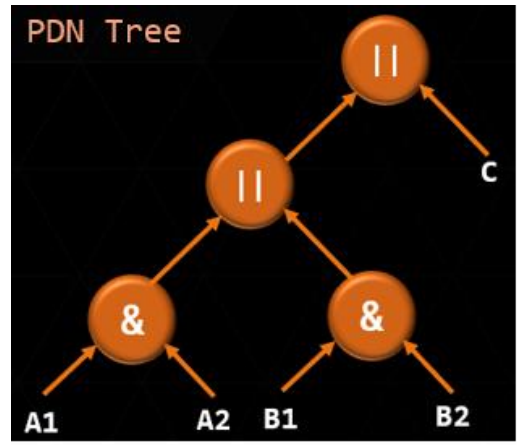
Challenges in MIS modelling

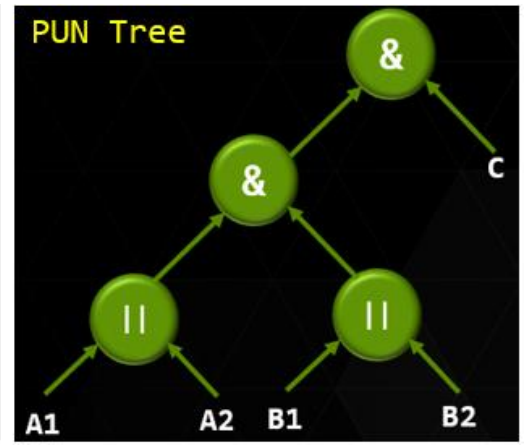
1. **Input Patterns**
    1. For multi-input cells like AOI, OAOI, MIS impact (speed-up or slow-down) depends on the input pattern.
    2. Speed-up/Slow-down depends on the state of the inputs: 0, 1, ↑,↓
    3. Lot of patterns to be simulated per lib-cell to find the worst MIS factor.
2. **Parameters**
    1. MIS speed-up/slow-down is proportional to input transition and output load.
    2. MIS increases with number of inputs for basic gates (AND/OR/NAND/NOR).
    3. MIS increases with cell drive strength.

Pattern Reduction Algorithm (PRA) for MIS

- Find the patterns that can cause worst MIS for each function. Use it for Spice simulation.
- Represent each logic function for Pull-up and Pull-down implementation in a binary tree.
- Leaves are operands, ancestors are operators.
- Two guiding rules:
  - Parallel NMOS/PMOS paths causes speed-up
  - Series NMOS/PMOS paths causes slow-down

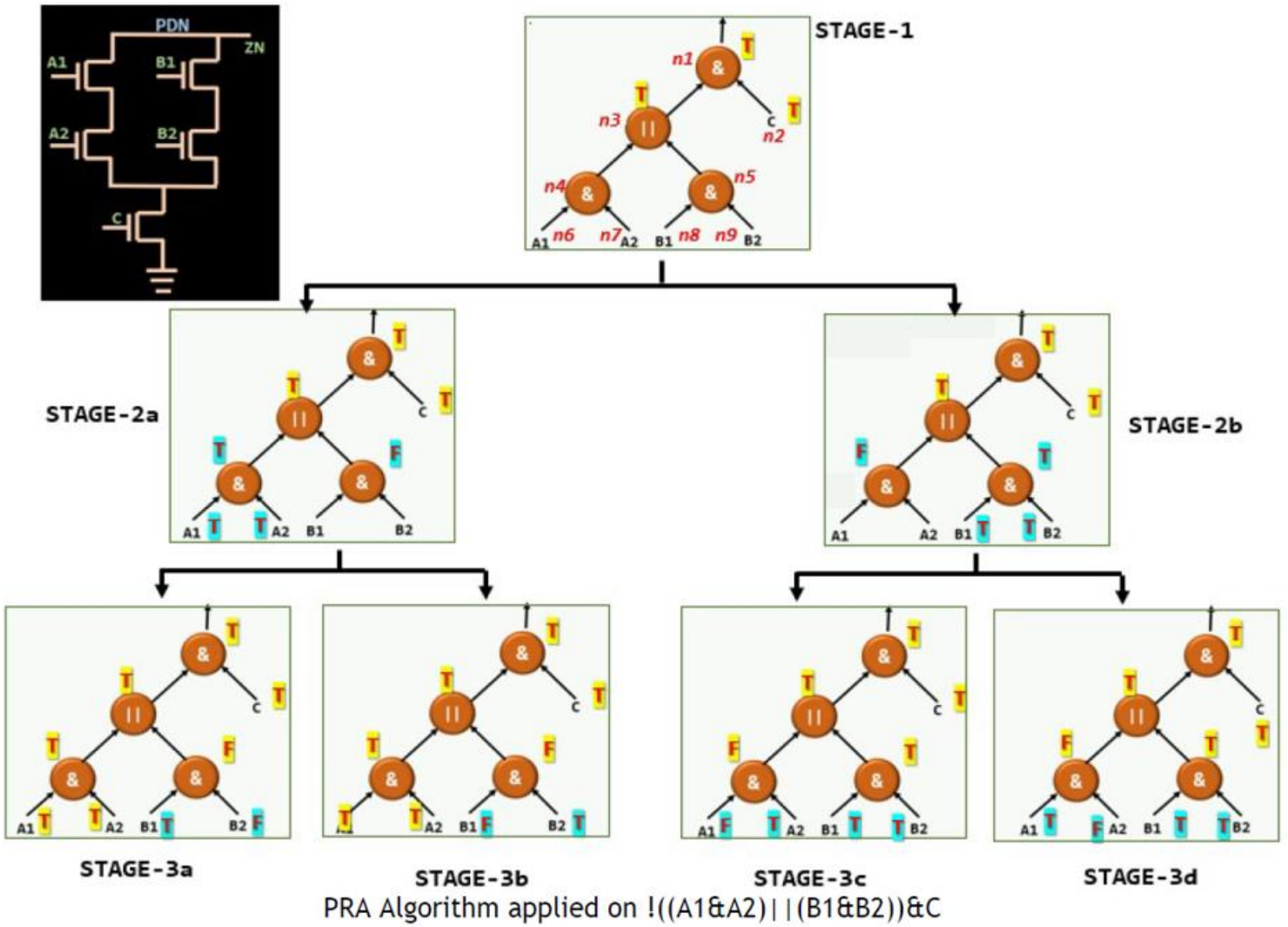






Proposal for MIS Characterization

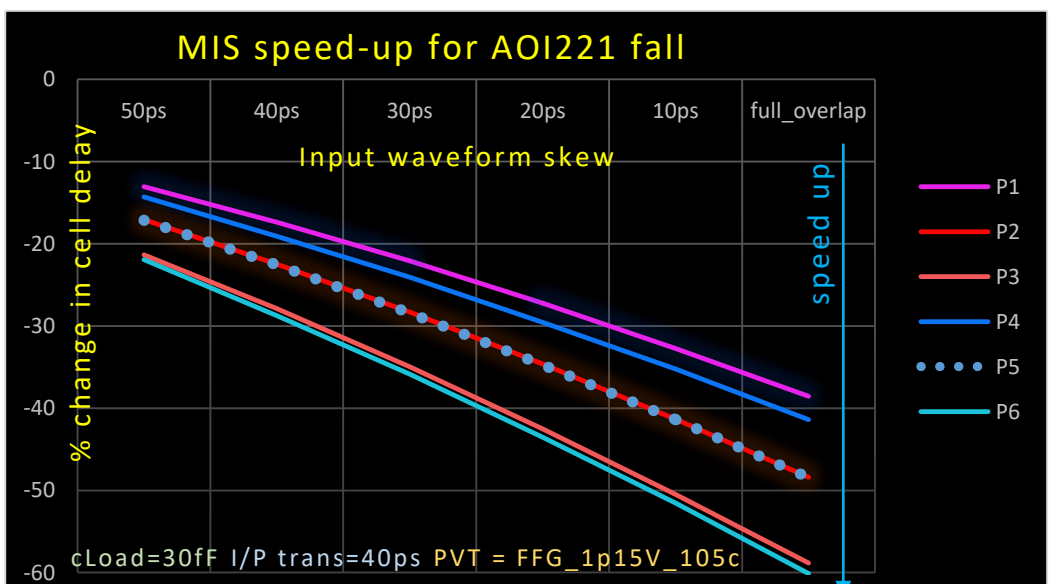
- Parse the binary tree to find the req. input pattern at other inputs for SIS at each input.
- Identify the inputs which can be potential MIS candidate from the SIS pattern.

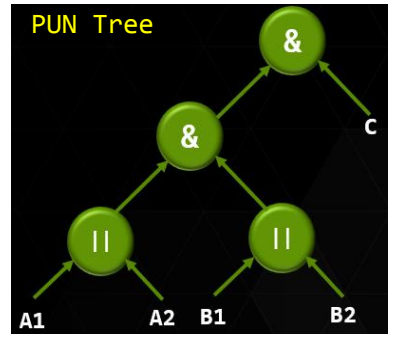


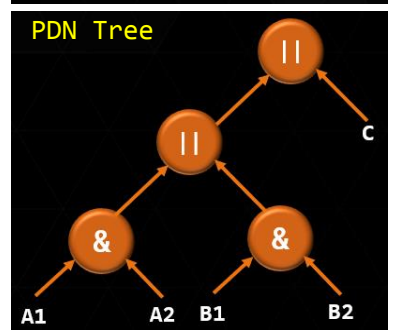
Results

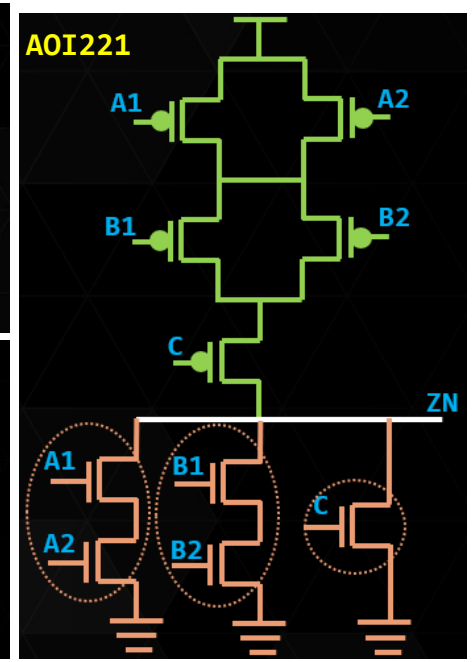
Pattern	Related Pin	SIS Condition					MIS impacting Pin	MIS Condition				
		A1	A2	B1	B2	C		A1	A2	B1	B2	C
P1	A1	↑	1	0	1	0	B1	↑	1	↑	1	0
P2							C			0	1	↑
P3							B1 and C			↑	1	↑
P4				1	0	0	B2			1	↑	0
P5							C			1	0	↑
P6							B2 and C			1	↑	↑

PDN speed-up patterns for A1 pin of AO1221



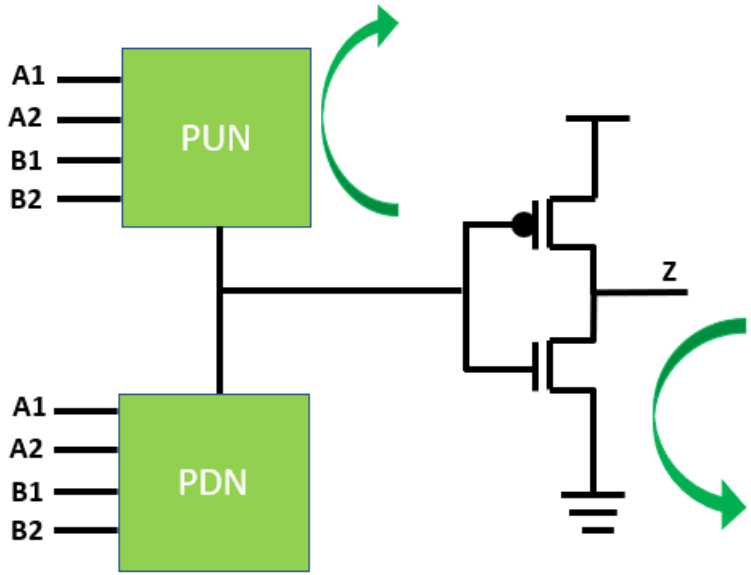






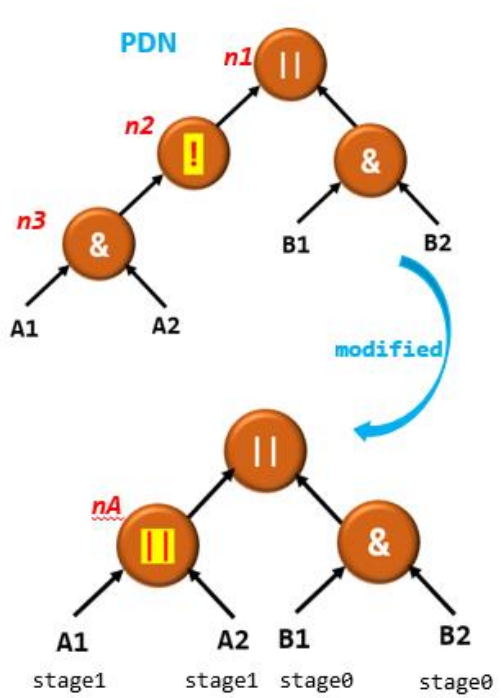
Handling Non-Inverting Logic

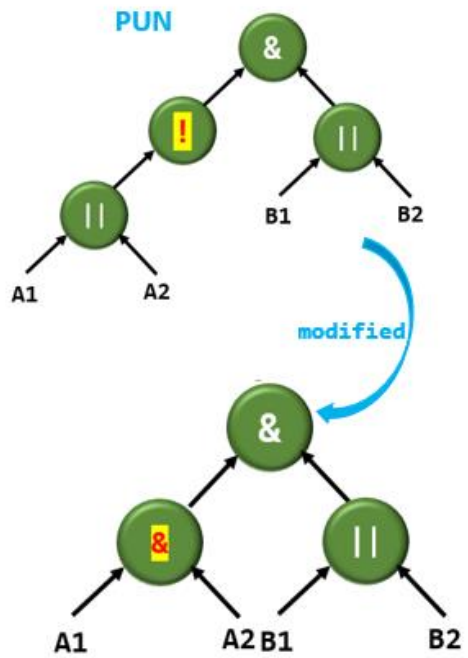
- Spice- Excitation:
  - For Fall MIS, the PUN need to be excited.
  - Hence, in Spice, PDN and PUN pattern need to be swapped.
- Spice-Measurement
  - For fall MIS, measurement Fall_at_input to Fall_at_output.

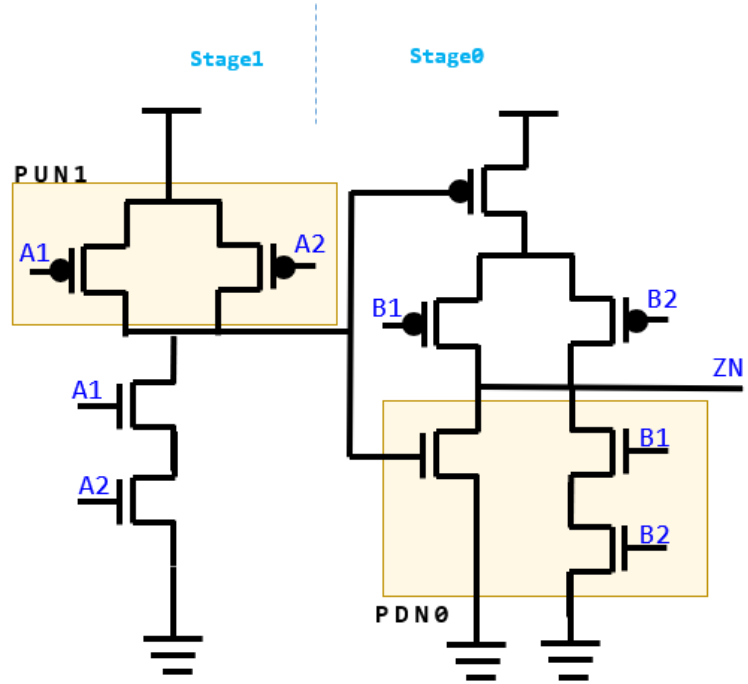


Handling Inversion with-in the logic: !((!(A1&A2))|(B1&B2))

- A1, A2 are in stage1.
- A1,A2 related output fall will trigger || PUN in stage 1



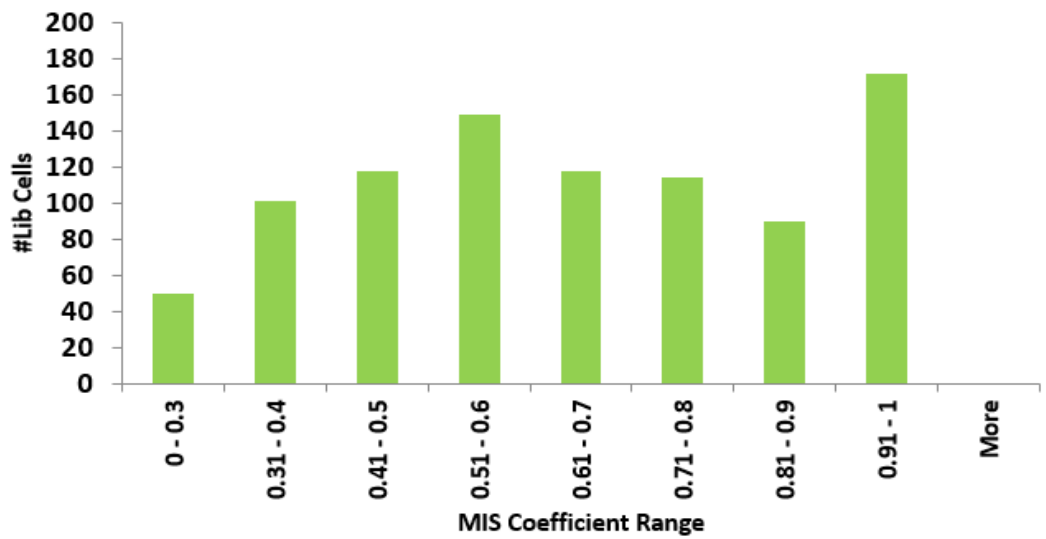


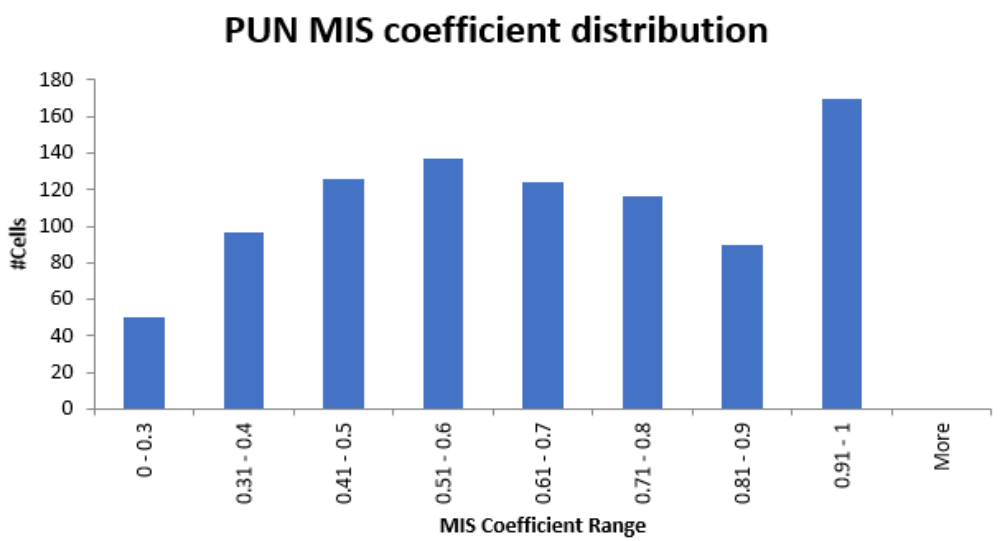


Results

STD CELL MIS Coefficients – 7nm/FFG_LV_HT

Function	Cell_name	PDN Coeff	PUN Coeff	PDN Detail Data				PUN Detail Data			
				Worst Coeff	Best Coeff	Diff	All Coeff	Worst Coeff	Best Coeff	Diff	All Coeff
(((A1&A2)|B)|C)	AO211D3	0.84	0.56	0.84	0.99	0.15	0.84 0.85 0.98 0.98 0.99 0.99	0.56	0.62	0.06	0.56 0.59 0.60 0.60 0.61 0.62
(!(((A1&A2)|B)|C))	AOI211D3	0.28	0.75	0.28	0.36	0.08	0.28 0.30 0.34 0.35 0.36 0.36	0.75	0.9	0.15	0.75 0.75 0.87 0.89 0.89 0.90



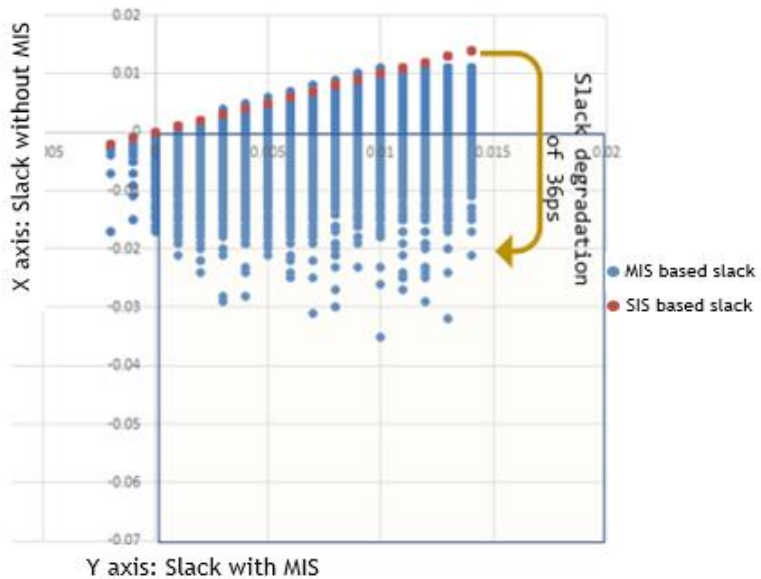


Results

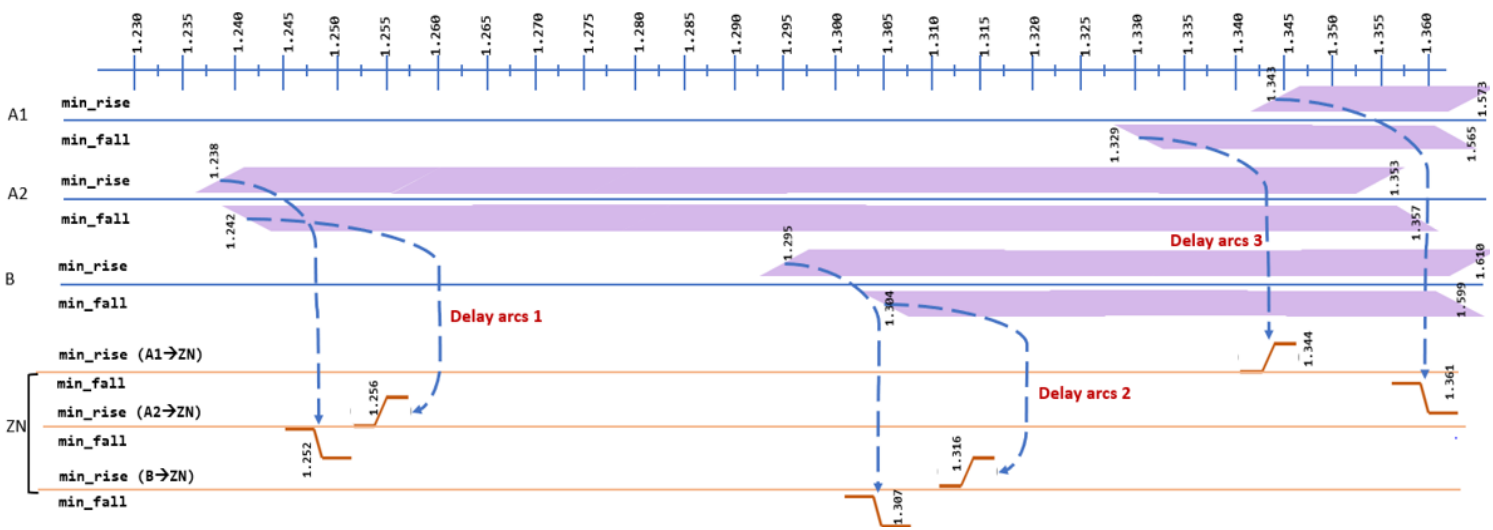
- Figure on bottom left shows the slack degradation when MIS is incorporated in STA tool. The bottom right quadrant shows the paths need to be reviewed for MIS impact and account 0.5% of paths in the design.

- A lot of these paths can be pruned, as datapath is too deep for them, and likelihood of input waveforms getting aligned for all cells on the path is very less. The inclusive pessimism is corrected based on path-depth. For realistic accounting, speed-up and slow-down both need to be included during setup and hold analysis.

- Another level of pessimism removal is shown in Fig on bottom right. For the rise/fall “Delay arcs 1”, when there is an A2→ZN transition, the input waveforms at pin A1 and B are not transitioning, hence there cannot be any MIS impact on A2→ZN delay.



MIS impact on STA of taped-out nVIDIA based design



Input pins window alignment for cell AOI21

Importance and Summary

- There is no industry standard method to quantify MIS, though the academic literature is rich, but impractical to implement.
- The MIS impact on cell delays and output transition compels MIS characterization for robust standard cell delay modelling.
- This would ensure reduced pre and post silicon miscorrelation and thus contributing to silicon yield. Also, the margin pessimism in design presently covering for MIS can be reduced.
- The deterrence to incorporate MIS into STA has been the intensive computation and data overhead that need to be added to the library.
- The novelty of the present work lies in reducing computational complexity and MIS coefficient database. The PRA algorithm helps identifying both speed-up and slow-down while the state-of-the-art EDA tools address only speed-up. PRA stands effective when EDA moves from MIS characterization of library to finding MIS derates during timing analysis.