The TAU 2019 Contest on Design Optimization

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Jignesh Shah
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The TAU 2019 Contest

Design Optimization Contest

George Chen
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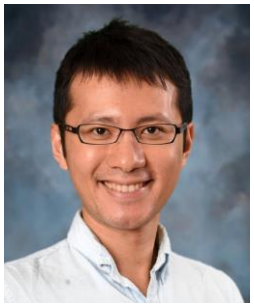
[Speaker]



Tsung-Wei Huang
University of Illinois at Urbana-Champaign

Jignesh Shah
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Sponsors:

Design Optimization

Why?

- Explore opportunities and limitations of optimizations as part of static timing analysis
- Explore incrementality and parallelism of optimizations within static timers

Allowed Optimizations

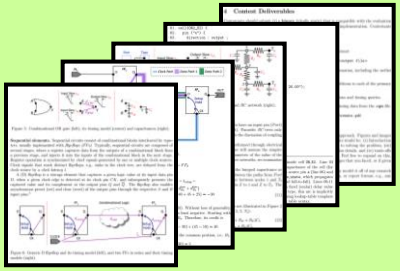
- Buffer insertion or deletion
- Buffer re-sizing

Contest Overview

Leveraged past TAU Timing Contest Infrastructure

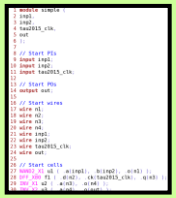
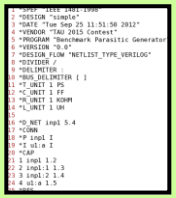
Provided to Contestants

Detailed Documentation



Timing and path reporting tutorials, file formats, timing model basics, evaluation rules, etc.

Benchmarks

Design Connectivity	Early and Late Libraries	Design Parasitics
		
Verilog (`.v`)	Liberty (`.lib`)	SPEF (`.spef`)

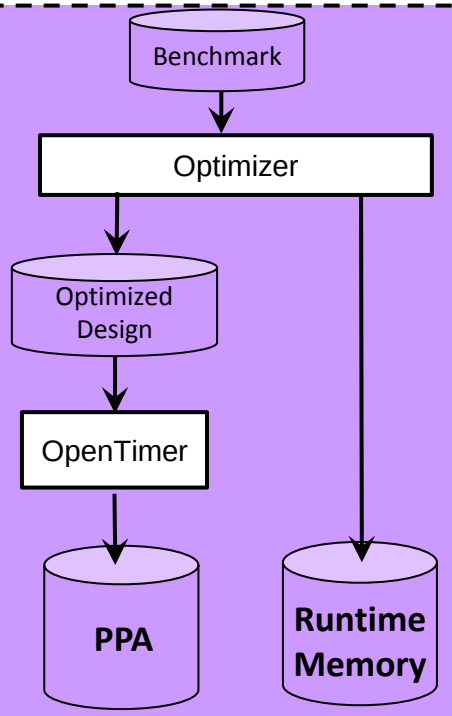
wrapper file (`.tau2019`)

Open Source Code and Binaries

1. *PATMOS 2011*: NTU-Timer
2. *TAU 2013*: IITiMer
3. *TAU 2014*: UI-Timer
4. *ISPD 2013*: .spef/.lib parsers
5. *TAU 2015 binary*: iTimerC v2.0
6. *OpenTimer* (UI-Timer v2.0)

Previous contest winners, utilities

Evaluation Method



Time frame: 11/1/2018 to 2/22/2019

Contest scope: Design Optimization

Benchmarks

Based on TAU 2015 Benchmarks

Design	Gates
s1196	641
systemcdes	3441
usb_funct	15,743
vga_lcd	139,529
leon2_iccad	795,371
leon3mp_iccad	659,017

Used Nangate FreePDK45 Generic Open Cell Library

- Contains area and power information

Evaluation Metrics

Overview

Metric	Weight	Remarks
Performance	100 pts	Max Clock Frequency
Power	50 pts	
Area	50 pts	
Runtime	70 pts	Elapsed time (not user time)
Memory	30 pts	Peak memory usage, including allocated memory
Documentation	100 pts	Clear description of algorithm and features
Total Points	**400 pts**	

Detailed Scoring Algorithm (400 points possible)

$$\text{Performance} = 100 * \frac{best\ clock\ period}{clock\ period}$$

$$\text{Power} = 50 * \frac{best\ power}{power}$$

$$\text{Area} = 50 * \frac{best\ area}{area}$$

$$\text{Runtime} = 70 * \frac{best\ runtime}{runtime}$$

$$\text{Memory} = 30 * \frac{best\ memory}{memory}$$

TAU 2019 Contestants

	University	Team
 	National Chiao Tung University / National Taiwan University	iTimerP
	University of Illinois at Urbana-Champaign	LAB408
	Federal University of Santa Catarina	Ophidian
 	University of Texas at Austin/ Yale University	Parallel Closure
	Democritus University of Thrace (Xanthi, Greece)	TimeBoost

(Total teams initially signed up: 10)

Contestant Presentations

Contestant Presentations

A. *ParallelClosure: A Parallel Design Optimizer for Timing Closure* (Yi-Shan Lu)

B. *iTimer* (Hsien-Han Cheng)

C. *TimeBoost: Fine-Grained Interleaving of Multithreaded Lagrange Relaxation based Gate Sizing with Buffering Optimizations* (Apostolos Stefanidis)

Results

Performance

	fast corner			typical corner		
Best Period (ps)	**Team A**	**Team B**	**Team C**	**Team A**	**Team B**	**Team C**
s1196	191	312	339	334	588	558
systemcdes	469	835	812	695	1403	1260
usb_funct	618	1030	1386	927	1726	1954
vga_lcd (no spef)	427	3214	TLE	684	7197	TLE
leon2_iccad (no spef)	892	TLE	TLE	1483	TLE	TLE
leon3mp_iccad	1000	TLE	TLE	1661	TLE	TLE

Power

	fast			typical		
Power under Best Period	**Team A**	**Team B**	**Team C**	**Team A**	**Team B**	**Team C**
s1196	44,686	51,079	47,604	12,968	12,605	13,646
systemcdes	288,976	320,212	2,212,020	83,265	103,240	605,271
usb_funct	1,577,190	2,239,540	118,070,000	449,515	560,749	31,699,900
vga_lcd (no spef)	10,807,000	4,074,340	TLE	3,125,270	4,119,360	TLE
leon2_iccad (no spef)	104,897,000	TLE	TLE	30,442,300	TLE	TLE
leon3mp_iccad	82,102,100	TLE	TLE	23,685,800	TLE	TLE

Area

	fast			typical		
Area under Best Period	**Team A**	**Team B**	**Team C**	**Team A**	**Team B**	**Team C**
s1196	592	671	620	592	591	618
systemcdes	3799	4703	14133	3799	4982	14141
usb_funct	20624	33525	623711	20624	31709	618484
vga_lcd (no spef)	146758	226993	TLE	146758	228850	TLE
leon2_iccad (no spef)	1312360	TLE	TLE	1312360	TLE	TLE
leon3mp_iccad	1028210	TLE	TLE	1028210	TLE	TLE

Runtime

cpu runtime (s)	Team A	Team B	Team C
s1196	1	17	1
systemcdes	18	494	9
usb_funct	96	1280	2307
vga_lcd (no spef)	45	9435	TLE
leon2_iccad (no spef)	366	TLE	TLE
leon3mp_iccad	242	TLE	TLE

Memory

memory (M)	Team A	Team B	Team C
s1196	45	297	124
systemcdes	86	313	552
usb_funct	209	511	1365
vga_lcd (no spef)	638	1778	TLE
leon2_iccad (no spef)	7290	TLE	TLE
leon3mp_iccad	6030	TLE	TLE

Scoring

Scoring	Possible Score	Team A	Team B	Team C
Performance	100	100	42	41
Power	50	50	42	13
Area	50	50	38	16
Runtime	70	61	19	18
Memory	30	30	6	3
Documentation	100	100	95	90
Total Score	**400**	**391**	**242**	**181**

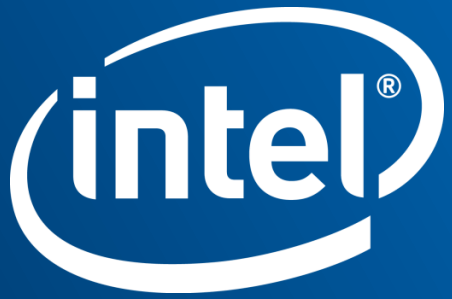
Acknowledgements and Announcements

Acknowledgements

- Song Chen, Workshop General Chair
  - Handling logistics for the contest
- TAU 2019 Contestants
  - All the great questions and hard work

Announcements

- TAU 2020 Contest Co-Chairs:
  - Jignesh Shah, Intel Corp
  - Tsung-Wei Huang, University of Illinois at Urbana-Champaign
- Looking for volunteers to participate on the TAU 2020 Contest Committee!


intel

TAU 2019

Timing Contest on Design Optimization

3rd Prize

Presented to

Yi-Shan Lu, Wenmian Hua,

Ranjit Manohar, and Keshav Pingali

For

Parallel Closure

University of Texas at Austin
Yale University

George Chen	*Song Chen*	*João Geada*
Contest Chair	General Chair	Technical Chair

TAU 2019

Timing Contest on Design Optimization

2nd Prize

Presented to

Apostolos Stefanidis, Dimitrios Mangiras,

and Giorgos Dimitrakopoulos

For

Time-Boost

Democritus University of Thrace

Xanthi, Greece

George Chen	*Song Chen*	*João Geada*
Contest Chair	General Chair	Technical Chair

TAU 2019

Timing Contest on Design Optimization

1st Prize

Presented to

Hsien-Han Cheng, Tung-Wei Lin, Yu-Cheng Lin
Iris Hui-Ru Jiang, and Pei-Yu Lee

For

iTimerP

National Chiao Tung University
National Taiwan University

George Chen	*Song Chen*	*João Geada*
Contest Chair	General Chair	Technical Chair