SYNOPSYS®
Silicon to Software™

Simultaneous Multi Voltage Analysis with Dynamic Voltage Frequency Scaling

Paul Berevoescu

Agenda

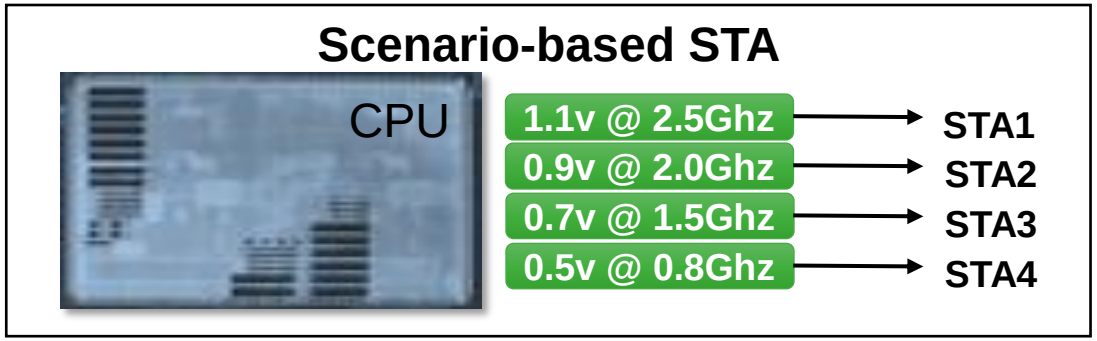
- Motivation
- Existing Simultaneous Multi Voltage Analysis methodologies
  - In-depth flow and compute resource review
- Optimized Simultaneous Multi Voltage Analysis
  - Detailed overview
  - Solution application
  - Results
- Summary

Definitions/Terminology

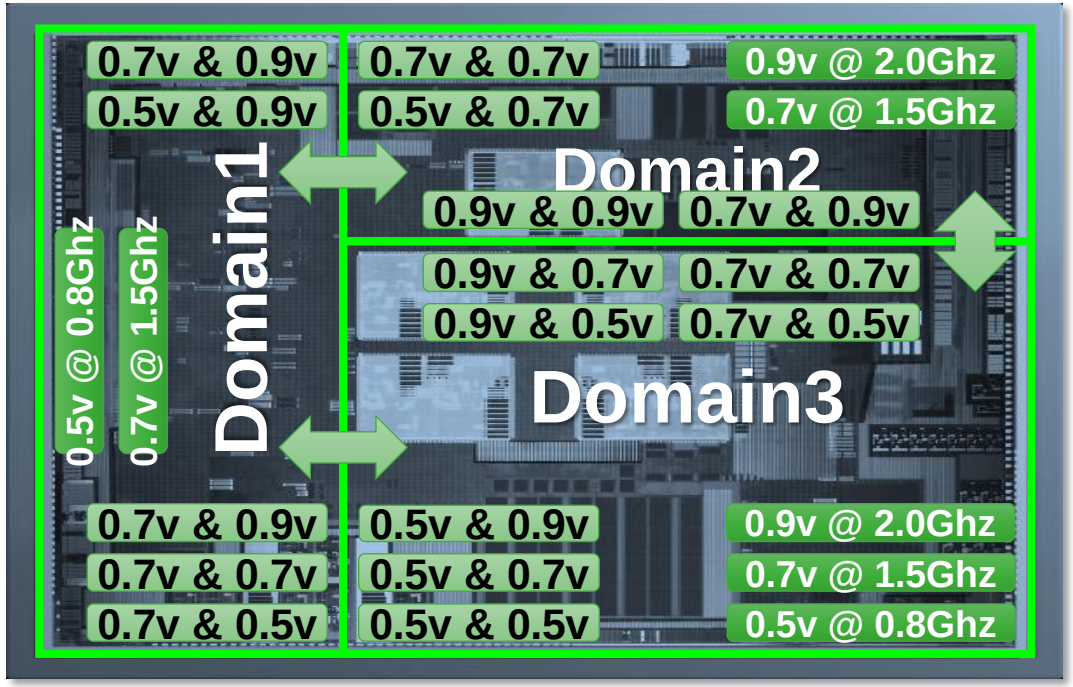
- SMVA = Simultaneous Multi Voltage Analysis
  - Applications
    - Analysis of voltage supply variation for designs with multiple voltage domains
  - What
    - Clock frequency and other constraints are voltage independent
- DVFS = Dynamic Voltage Frequency Scaling
  - Applications
    - Analysis of designs that run at multiple voltage-clock frequency pairs
  - What
    - Voltage dependent Clock Frequency and relevant Timing Constraints and Path Exceptions
- DFVS + SMVA
  - Analyze both simultaneously

Existing SMVA with DVFS methodologies

Single Voltage Domain Analysis



Multiple Voltage Domain Analysis



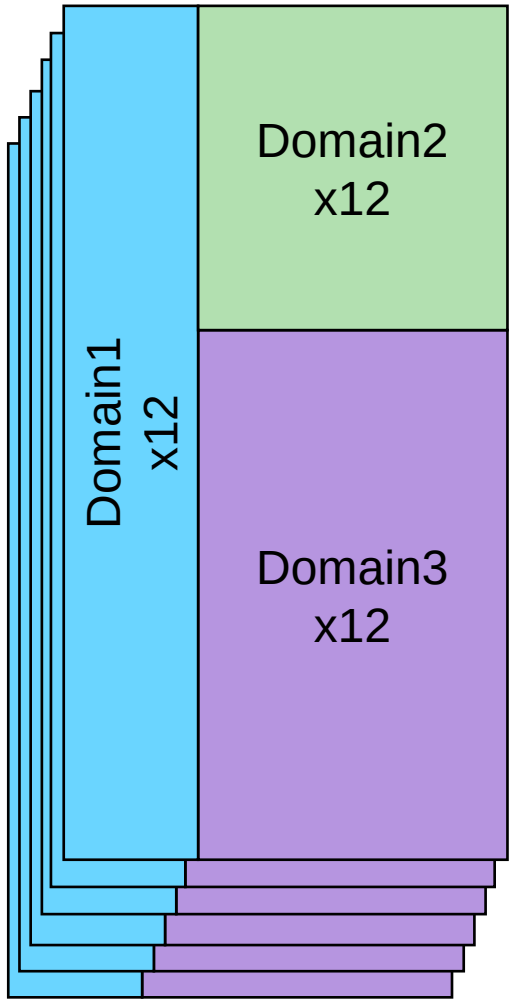
- Single Voltage Domain Analysis
  - *STA resources = **linear** = **f(Voltage Levels)***
- Multiple Voltage Domain Analysis
  - *STA resources = **exponential** =* $(\boldsymbol{Voltage\ Levels})^{(\boldsymbol{Voltage\ Domains})}$

Existing SMVA with DVFS Methodologies

Flow Resource Usage Analysis

M = # of voltage domains
N = max # of voltage levels in any voltage domain

Single corner, parallel runs solutions



Data input, pre STA
$O(N^M)$
x12

STA
$O(N^M)$
x12

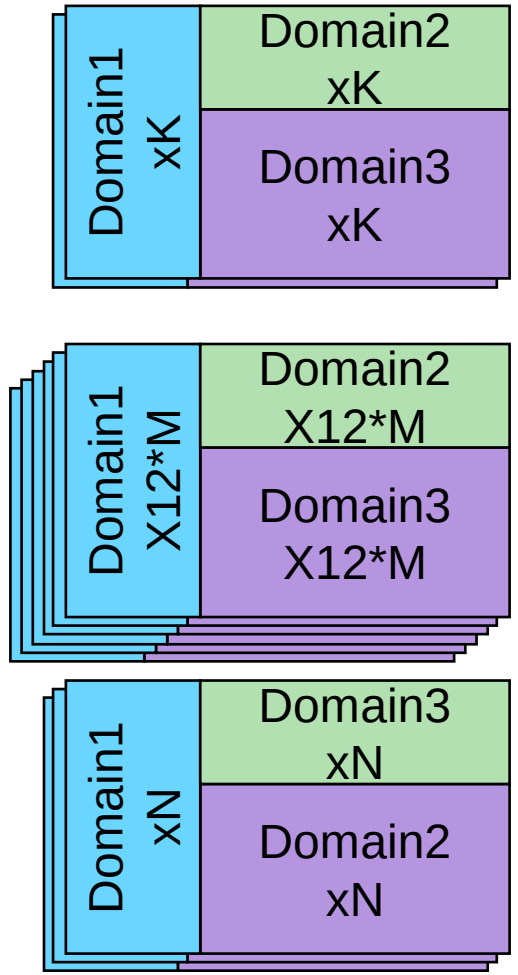
Post STA
$O(N^M)$
x12

Simultaneous Multi Scenario solutions

Data input, pre STA
O(1)
xK (K~1)

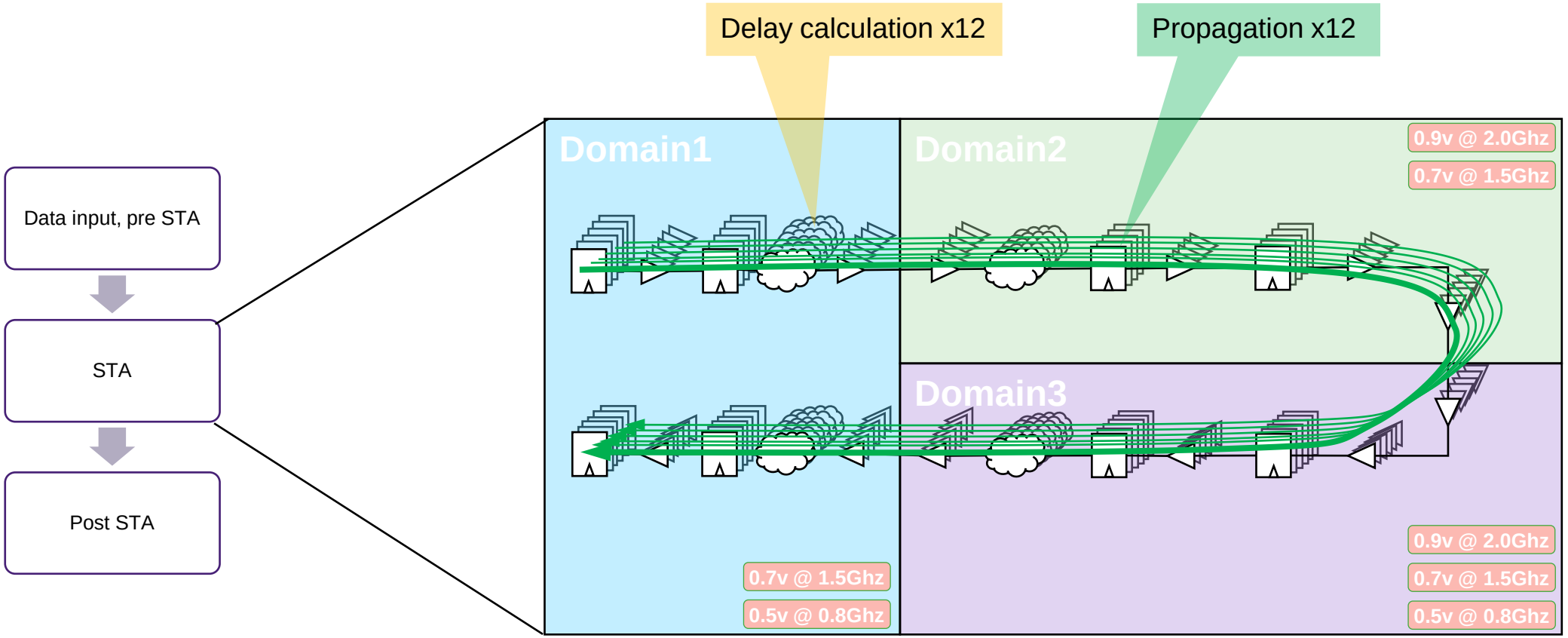
STA
$O(N^M)$
x12*M(M<=1)

Post STA
$O(N^M)$
xP(1<P<12)



Existing SMVA with DVFS Methodologies

STA Resource Usage Analysis

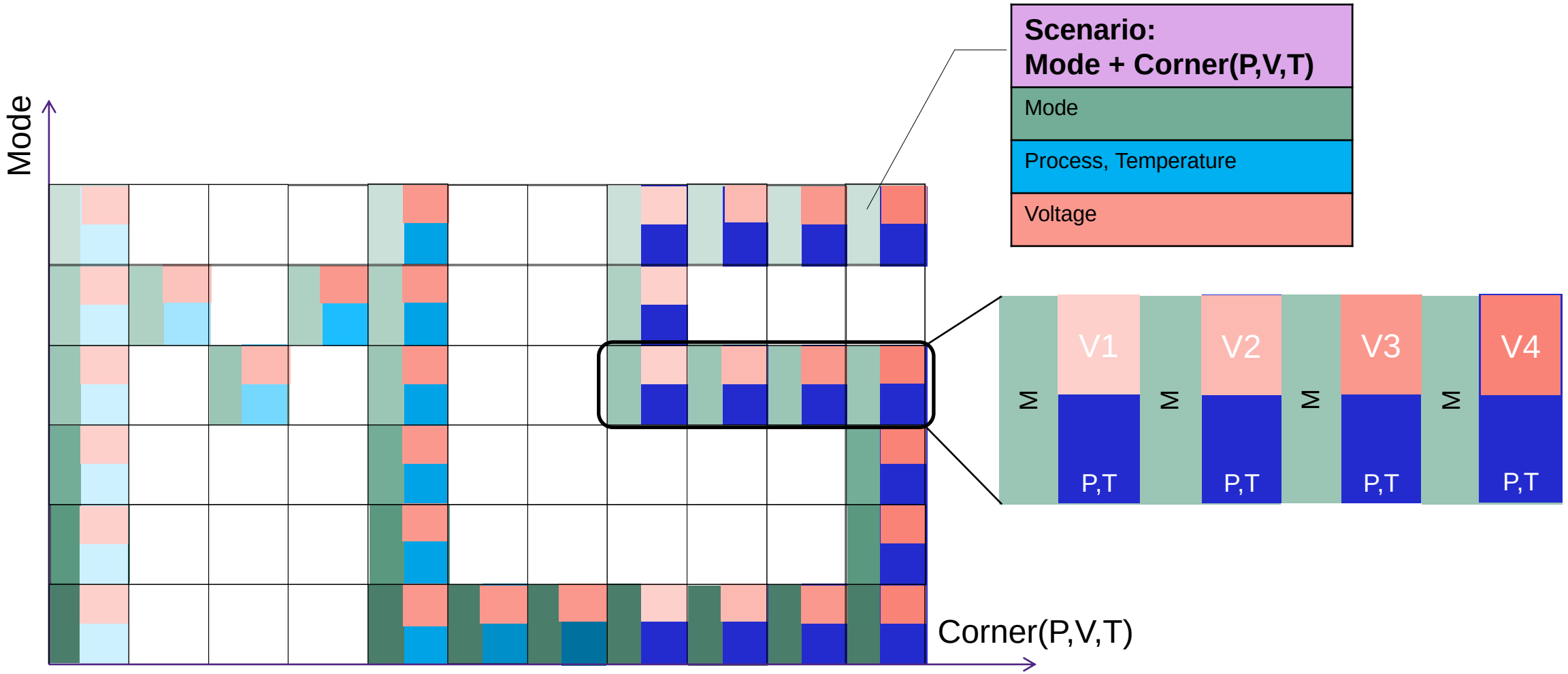


Existing SMVA with DVFS Methodologies

- Exponential exploration of voltage corners to cover all relevant voltage combinations
- Redundant front end: separate corner run flows redundantly process same netlist, same parasitics, same mode constraints
- Redundant analysis: per voltage scenario delay calculation and propagation at every cell
- Incomplete coverage: resource limitation = educated guess in selecting a sub-set of scenarios, potential issues remain unverified

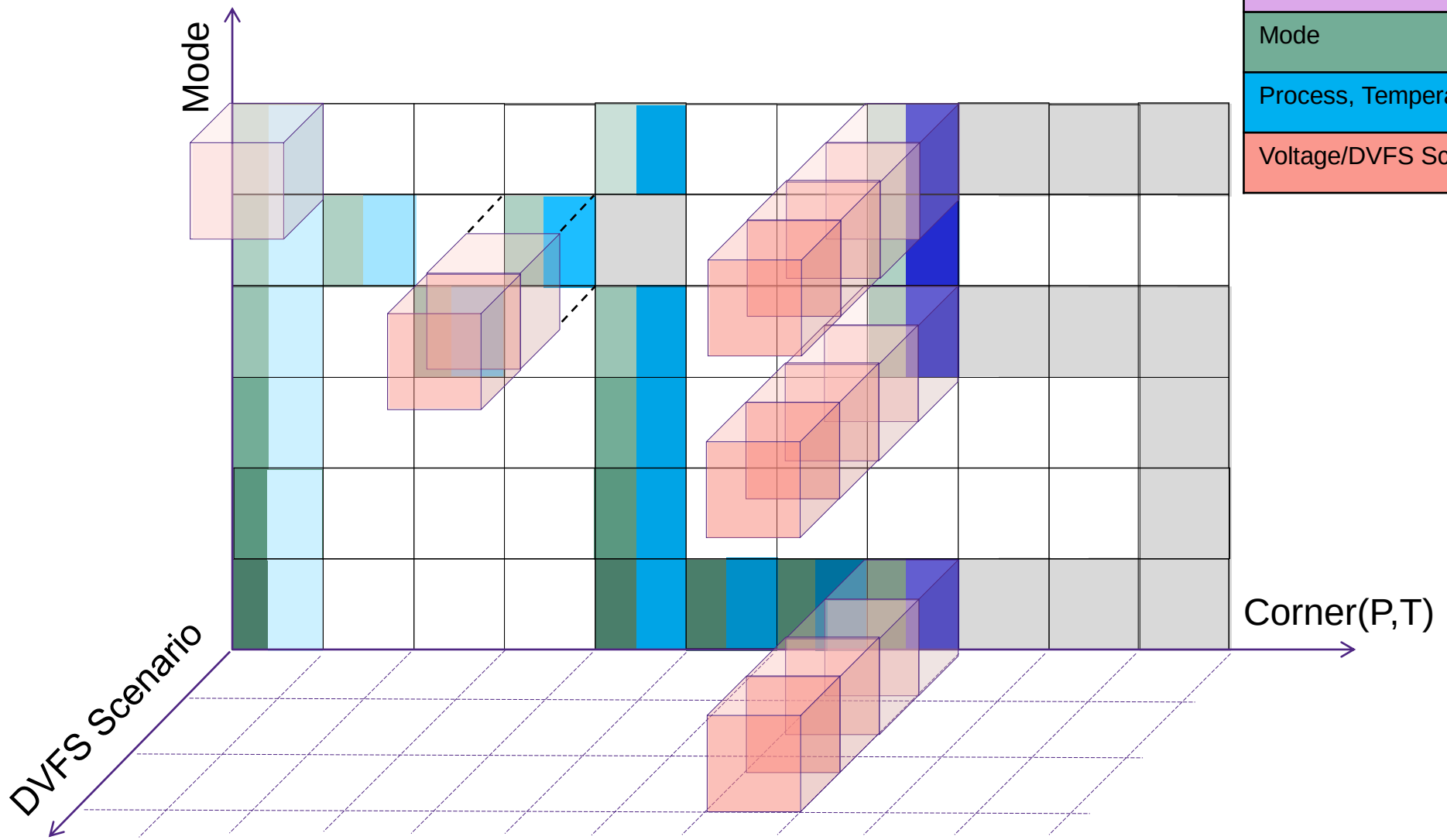
Existing SMVA with DVFS Methodologies

Traditional Multi Scenario Analysis Space



New SMVA with DVFS Methodology

3D Multi Scenario Analysis Space

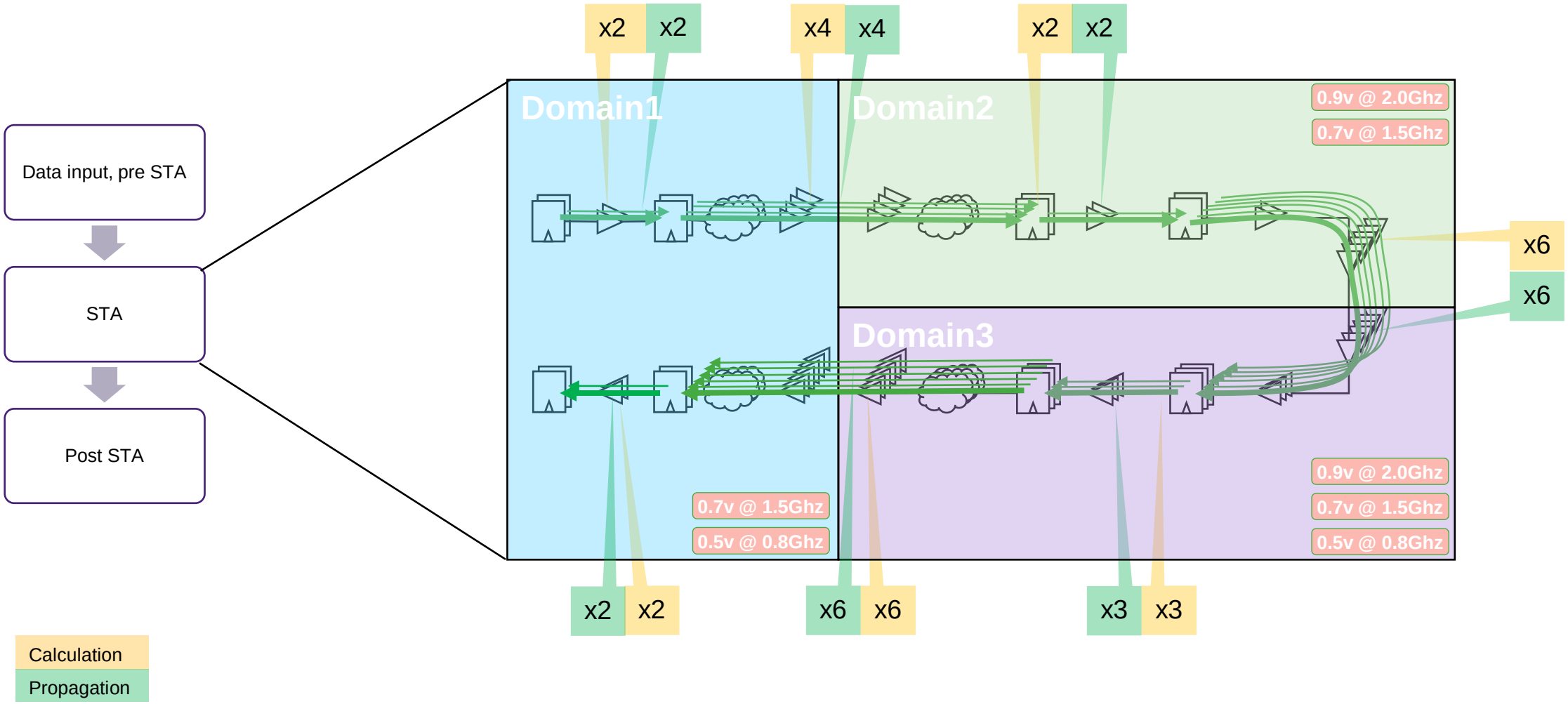


Scenario:
Mode + Corner(P,T) + DVFS Scenario

- Mode
- Process, Temperature
- Voltage/DVFS Scenario

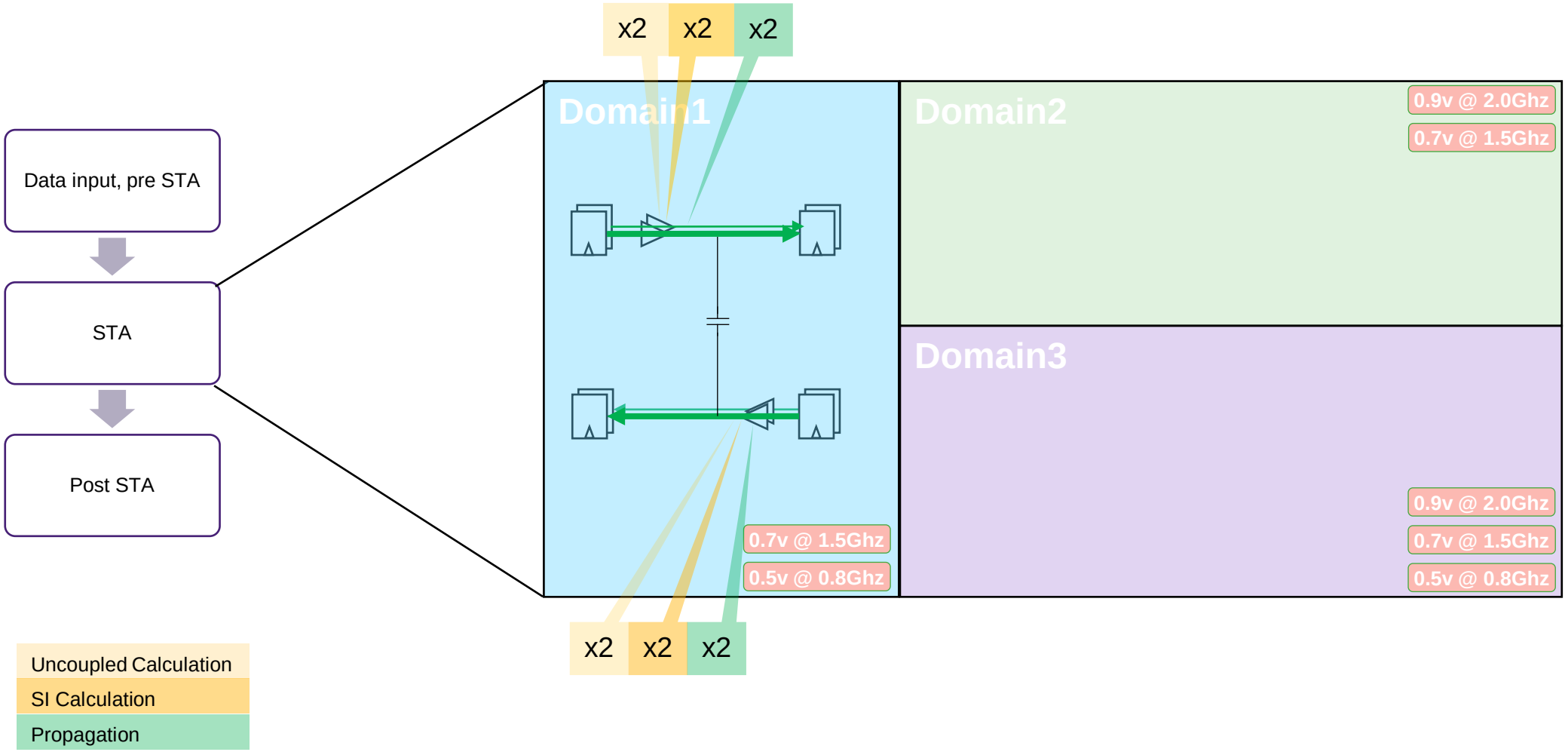
SMVA/DVFS Analysis

STA Resource Usage Analysis



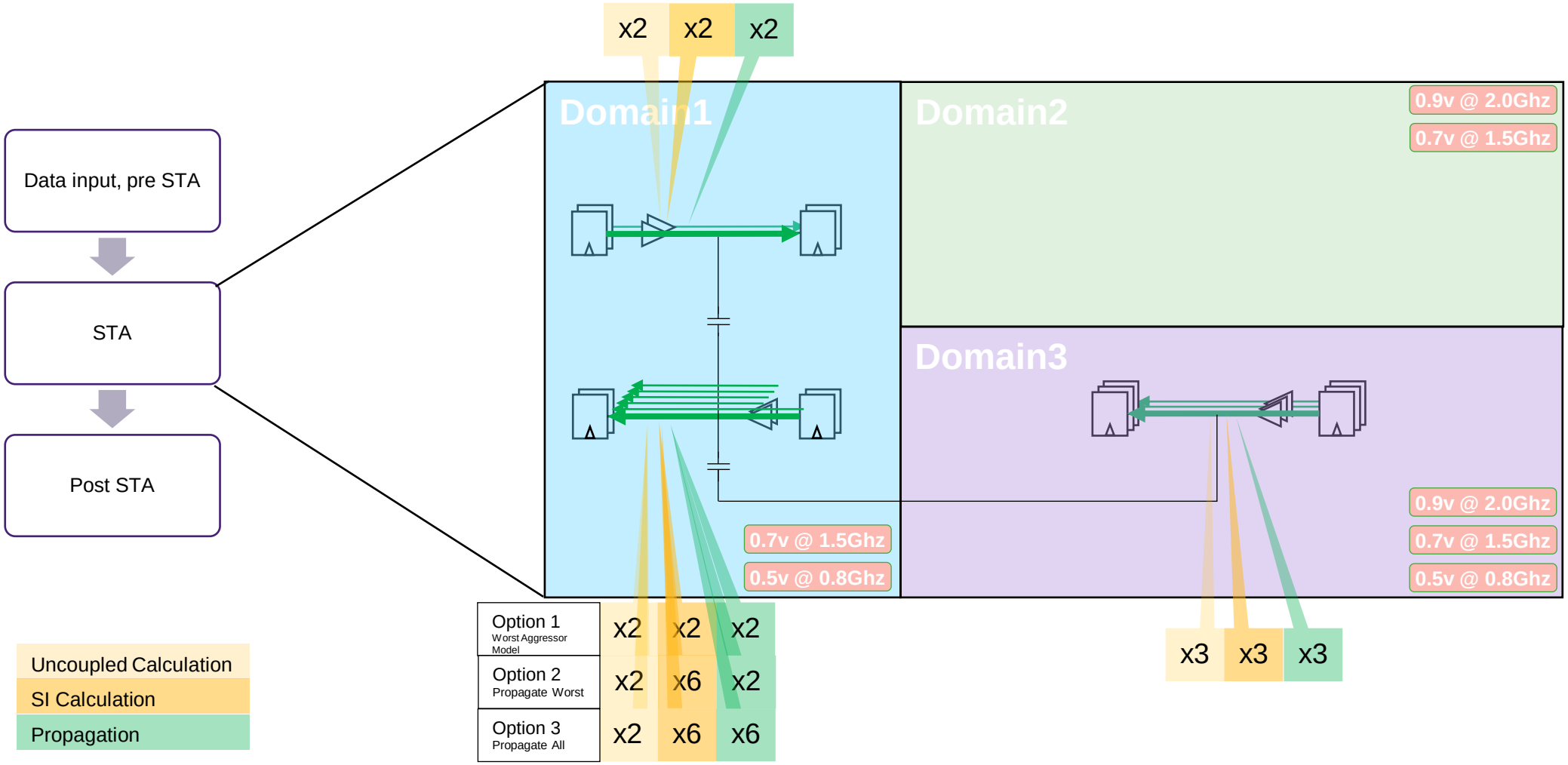
SMVA/DVFS Analysis

STA Resource Usage Analysis – SI, intra domain



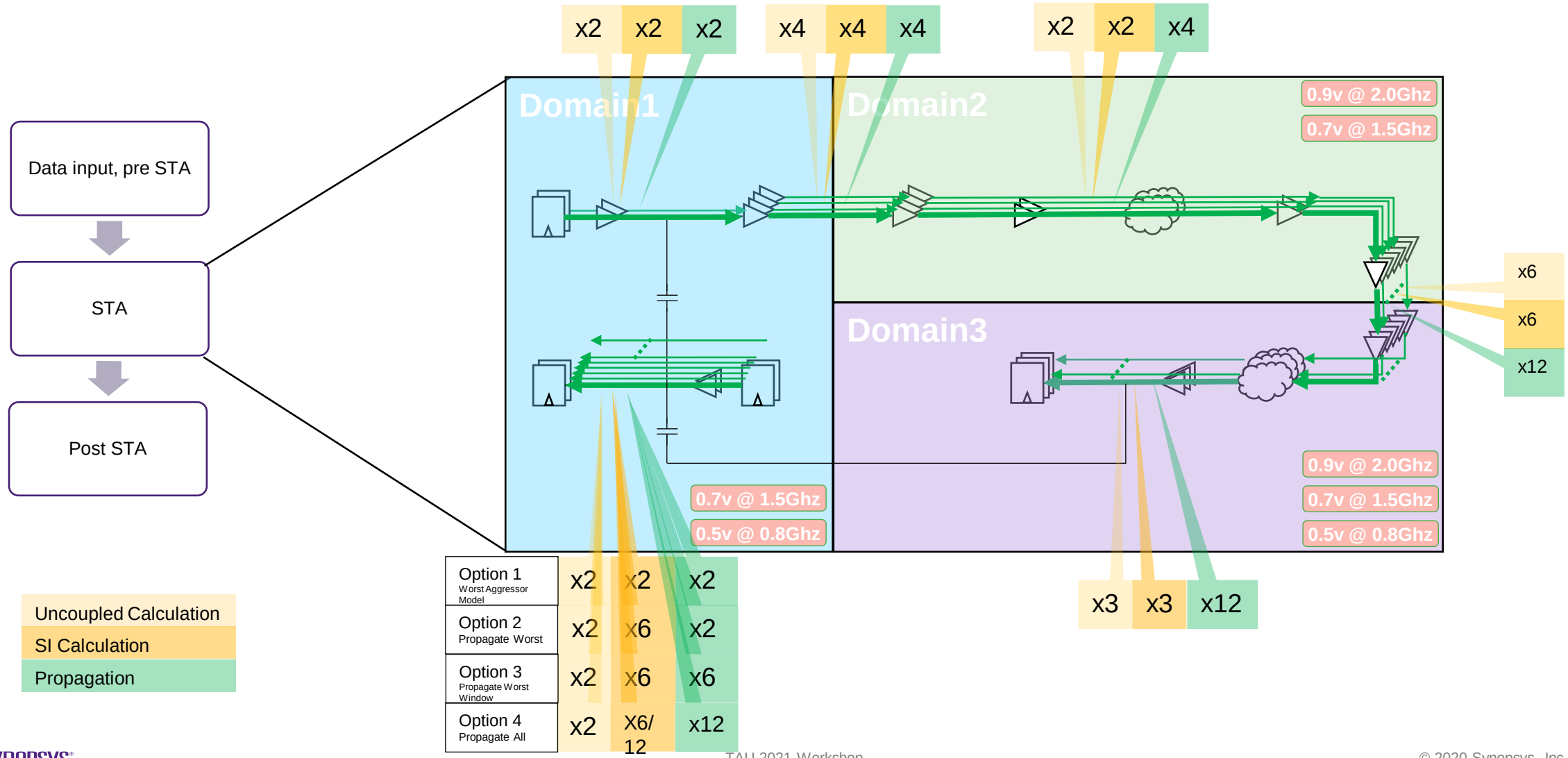
SMVA/DVFS Analysis

STA Resource Usage Analysis – SI – cross domain aggressor



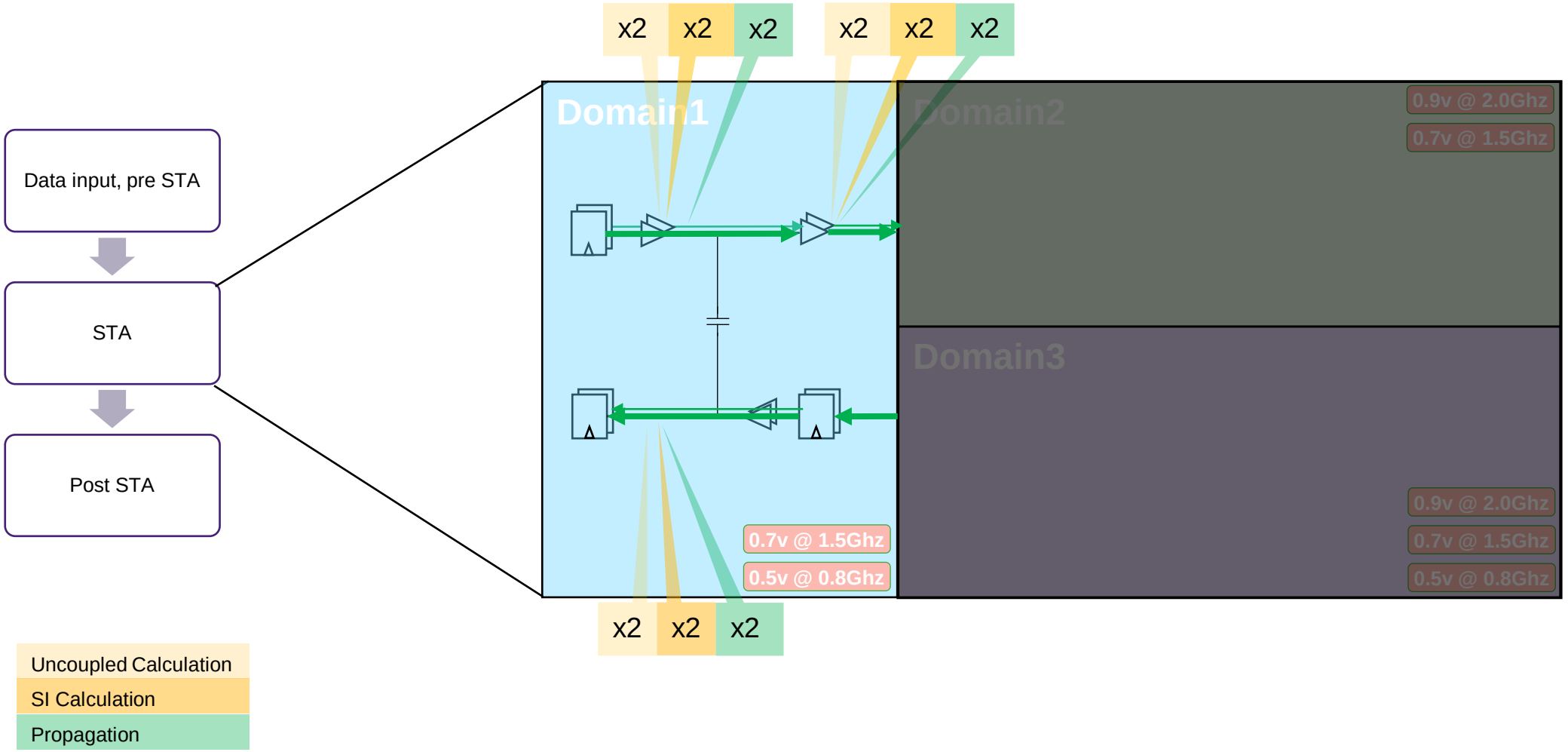
SMVA/DVFS Analysis

STA Resource Usage Analysis – SI – cross domain arrival window



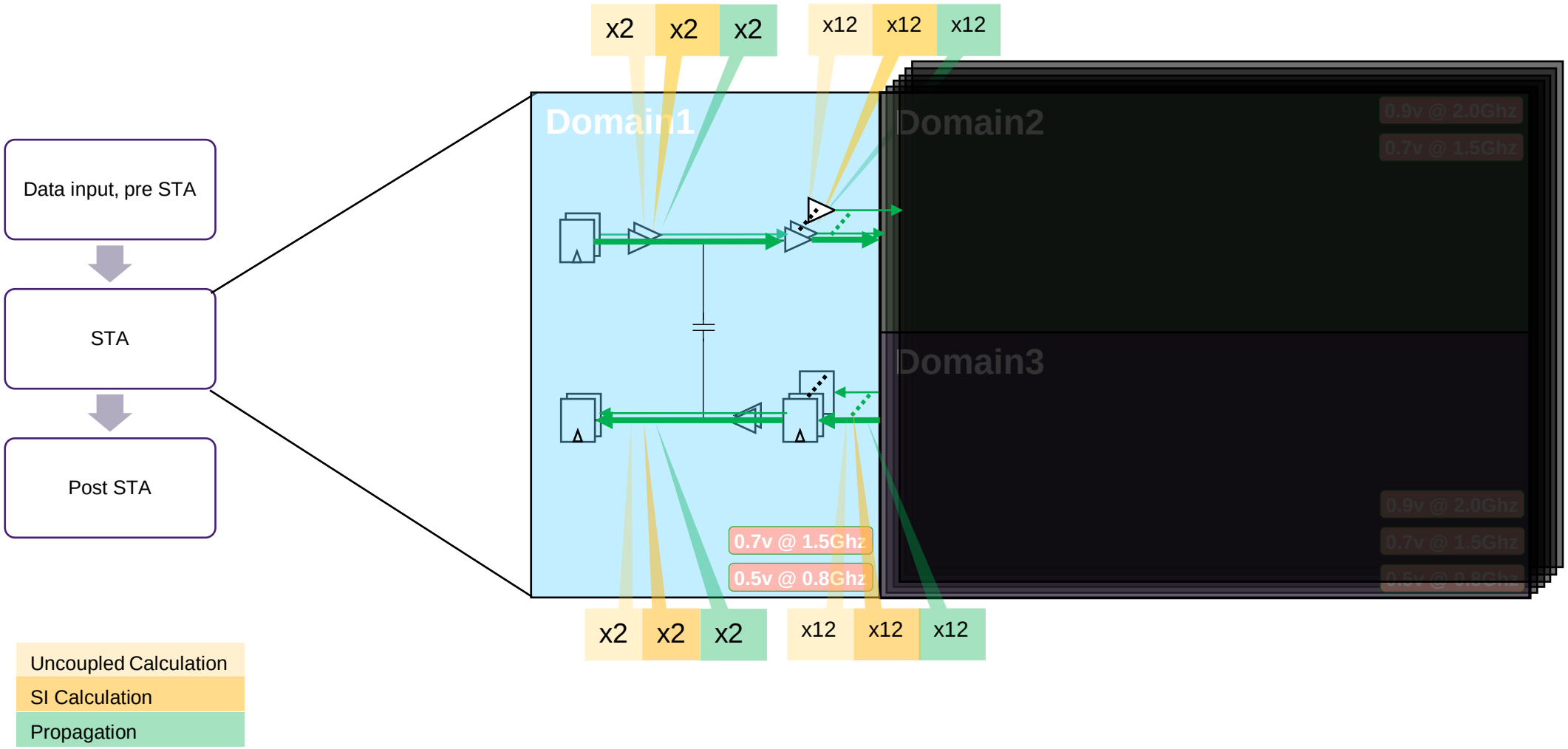
SMVA/DVFS Analysis

STA Resource Usage Analysis – Hierarchical flow – Worst case black box model



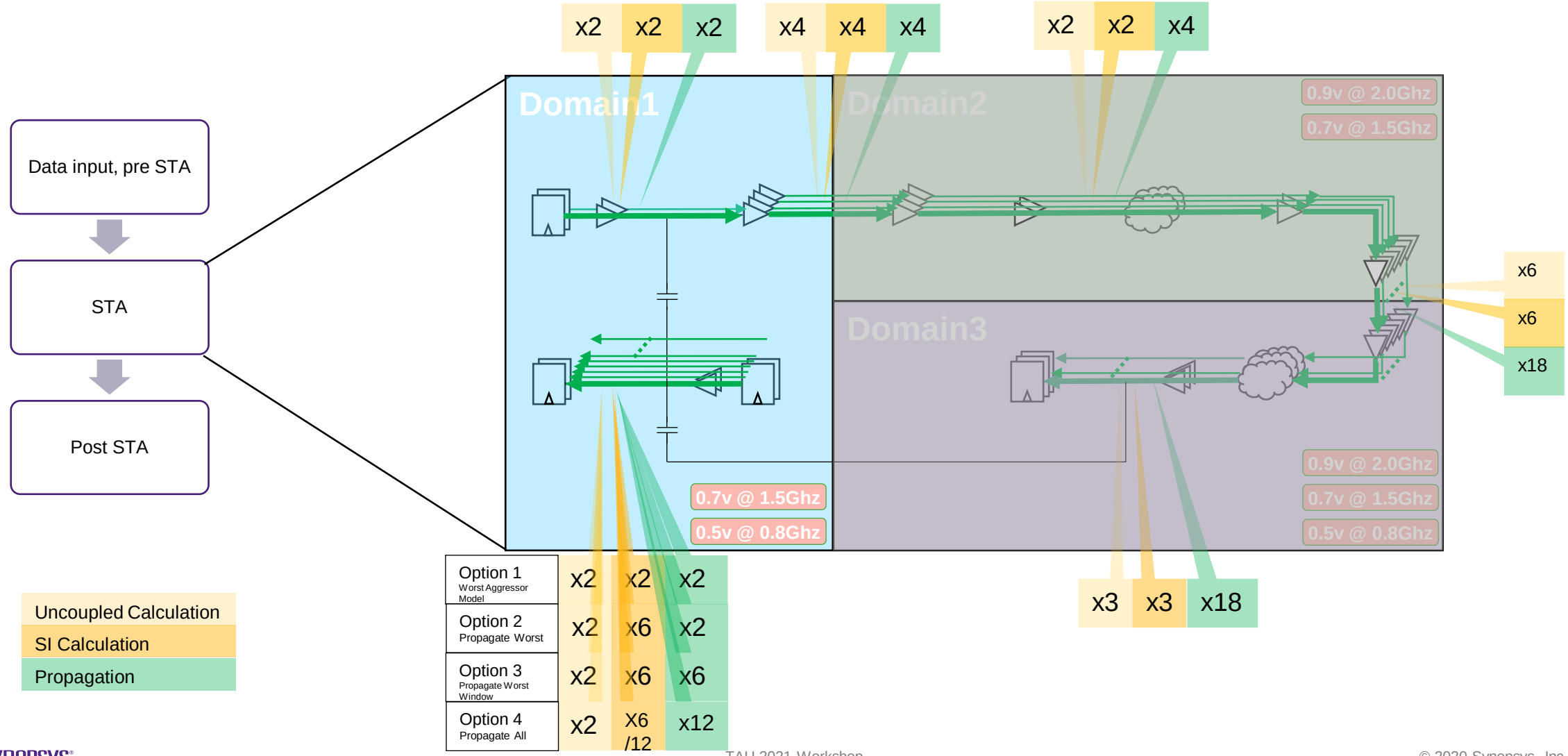
SMVA/DVFS Analysis

STA Resource Usage Analysis – Hierarchical flow – Enumerated black box model



SMVA/DVFS Analysis

STA Resource Usage Analysis – Hierarchical flow – SMVA/DVFS model

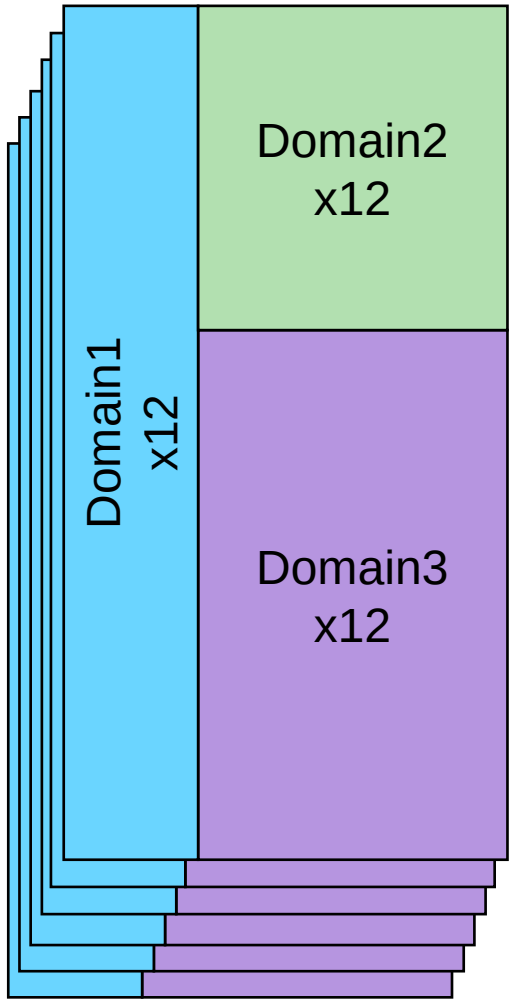


SMVA/DVFS Analysis

Flow Resource Usage Example

M = # of voltage domains
N = max # of voltage levels in any voltage domain

Single corner, parallel runs solutions



Data input, pre STA
$O(N^M)$
X12

STA
$O(N^M)$
x12

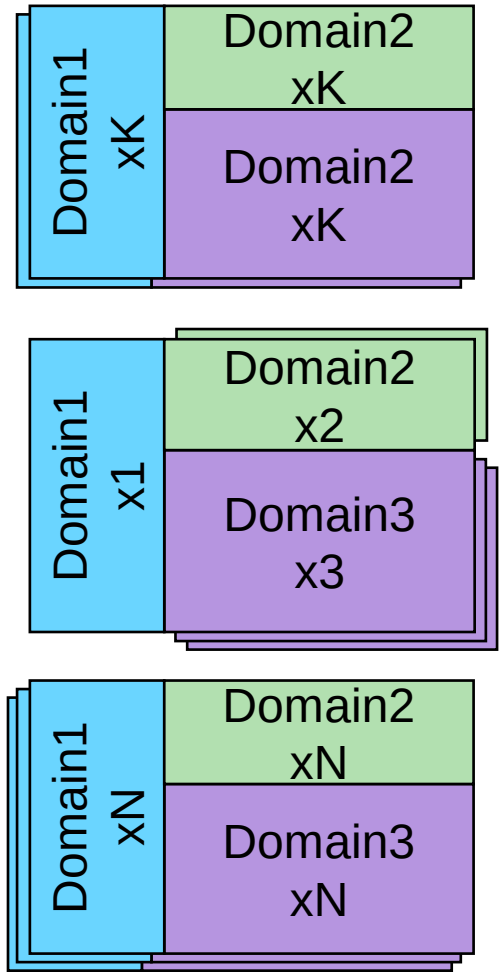
Post STA
$O(N^M)$
x12

Simultaneous Multi Scenario with DVFS

Data input, pre STA
$O(1)$
xK (K~1)

STA
$O(N)$
x3

Post STA
$O(N)$
xP(1<P<3)



Optimal SMVA/DVFS analysis

M = # of voltage domains
N = max # of voltage levels in any voltage domain

- Much improved Runtime/Memory compute resources utilization
  - Quasi linear *O(N),* with N = max # of voltage levels in any voltage domain
  - Compared to exponential $O(N^M)$ in traditional Simultaneous Multi Scenario flows
  - Memory typically less – large % of peak is pre analysis design data
  - Comprehensive analysis of all the relevant voltage combinations
    - Full analysis space coverage, no need to guess and hand pick signoff voltage corners

Optimal SMVA/DVFS analysis

Details

M = # of voltage domains
N = max # of voltage levels in any voltage domain

- *O(1)* pre timing analysis for same P,T corner and mode @ different voltages
- *O(N)* delay calculation and propagation for intra-domain paths
  - linear in max # of voltage levels
- *O(N)* delay calculation and *O(N^R)* propagation for cross-domain paths
  - 1 < R < 4 in most designs
  - small cross-domain paths % of all design paths
- *O(1)* post timing analysis @ worst case

Performance/Capacity

Corner/scenario reduction

Design	DVFS	Voltage setup		PT corners	Modes	Scenarios					
						All			Selected		
		# Voltage Domains	Max # Voltage Levels per Domain			W/O SMVA	With SMVA	Reduction	W/O SMVA	With SMVA	Reduction
1	N	6	2	21	7	9408	147	**64**			
	Y				2	9408	42	**224**			
2	N	7	2	15	20	38400	300	**128**	9600	300	**32**

Performance/Capacity Scaling with # Voltage Corners

SMVA Vs. Worst over Single Corners

- Design size: ~1M Instances
- Voltage domains: 2

SMVA Vs Corner	Full Flow						update_timing					
	Runtime			Memory			Runtime			Memory		
		SMVA Vs. 1 corner	SMVA Benefit		SMVA Vs. 1 corner	SMVA Benefit		SMVA Vs. 1 corner	SMVA Benefit		SMVA Vs. 1 corner	SMVA Benefit
1 corner	1,723 secs	1.0 x	1.0 x	14.2 GB	1.0 x	1.0 x	440 secs	1.0 x	1.0 x	2.6 GB	1.0 x	1.0 x
4 corners (SMVA)	2,376 secs	1.4 x	2.9 x	15.9 GB	1.1 x	3.6 x	1,020 secs	2.3 x	1.7 x	5.4 GB	2.1 x	1.9 x
9 corners (SMVA)	2,768 secs	1.6 x	5.6 x	17.5 GB	1.2 x	7.3 x	1,440 secs	3.3 x	2.8 x	7.0 GB	2.7 x	3.4 x
16 corners (SMVA)	3,306 secs	1.9 x	8.3 x	19.3 GB	1.4 x	11.7 x	1,860 secs	4.2 x	3.8 x	9.0 GB	3.4 x	4.7 x

Performance/Capacity

Design specific data

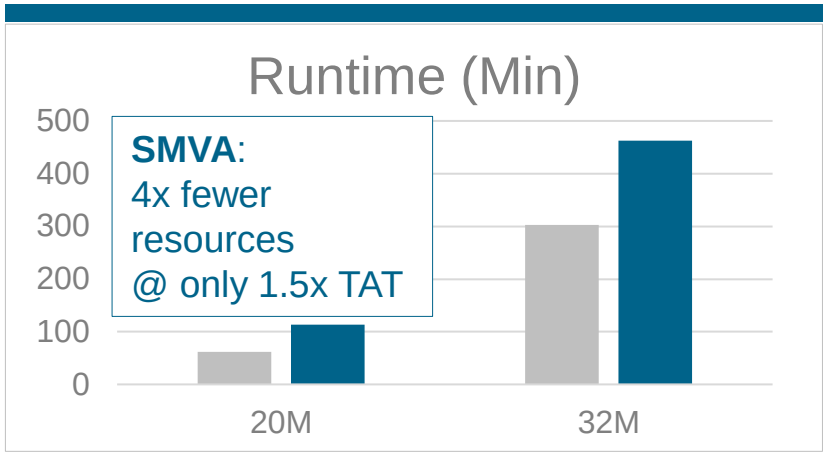
Designs	Stage	Elapsed Time (in mins)			Peak Memory (in GB)	
		Corner	SMVA	X-Factor SMVA/Corner	Corner	SMVA
Design1	STA	5.92	15.03	**2.5**	8.57	11.85
Design2	STA	0.05	0.08	**1.7**	3.72	3.73
Design3	STA	0.03	0.05	**1.5**	3.51	3.51
Design4	STA	1.42	2.82	**2.0**	7.30	7.92
Design5	STA	1.42	2.82	**2.0**	7.30	7.92
Design6	STA	78.62	155.43	**2.0**	35.03	49.89

Performance/Capacity

SMVA Vs. Worst over Single Corners

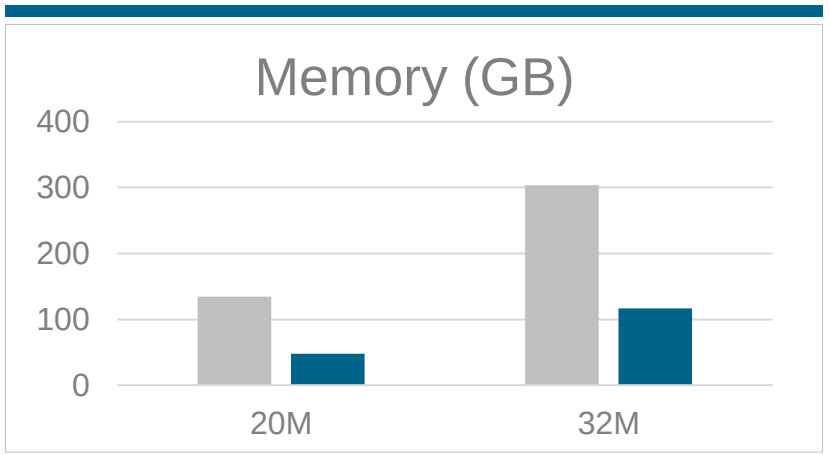
- Design size: ~20 M Instances (SI Flow)

Stage	Runtime (in mins)		
	Corner	SMVA	X-factor
Pre-STA	14	15	**1.1 x**
STA	48	99	**2.1x**
TOTAL	62	114	**1.8 x**



- Design size: ~32 M Instances (SI Flow)

Stage	Runtime (in mins)		
	Corner	SMVA	X-factor
Pre and post STA	195	193	**1.0 x**
STA	108	269	**2.5x**
TOTAL	303	462	**1.5 x**



Traditional: 2 domains, 2 levels (8 Cores each = 32 Cores in Single machine)

Summary

- Existing Multiple Voltage Domain Analysis STA solutions
  - Exponential compute resources – F(# of voltage cross combinations)

- New Multiple Voltage Domain Analysis STA solution
  - Re-defined 3D STA Analysis Space and constraints language for separate voltage dependency
  - New solution applies correlated voltage dependency both locally and path specific
  - Linear compute resources – F(max # of voltage levels)
  - Eliminates calculation and propagation redundancy caused by 2D STA Analysis Space limitations

Appendix

SMVA with DVFS STA compute resource estimation

General estimation formula: $\mathbf{R = r \times \sum_{i=0}^{m} \frac{p_i}{100} \times n_i}$ + XPO

- Given a design D with
  - m supply groups (power domains) $SG_{i,\ 0<i<=m}$, each constituting a percentage $p_{i,\ 0<i<=m}$ of the design logic
  - up to n_i voltage levels per domain SG_i: $L_{ij,\ 0<i<=m,\ 1<j<=ni}$
  - up to k voltage domain crossings for a small percentage $xp_{q,\ 1<q<=k}$ of the design paths
    - domain crossing paths constitute a small percentage xp% (usually less than 5%) of the total paths
    - paths crossing k domains are analyzed across n^k combinations
      - Only path propagation is affected – assume approximately 30% of STA
  - assuming r is the STA worst case runtime across all single voltage scenario runs

- General formula for estimating STA compute resource usage with the above definitions

$\mathbf{R = r \times \sum_{i=0}^{m} \frac{p_i}{100} \times n_i}$ + XPO

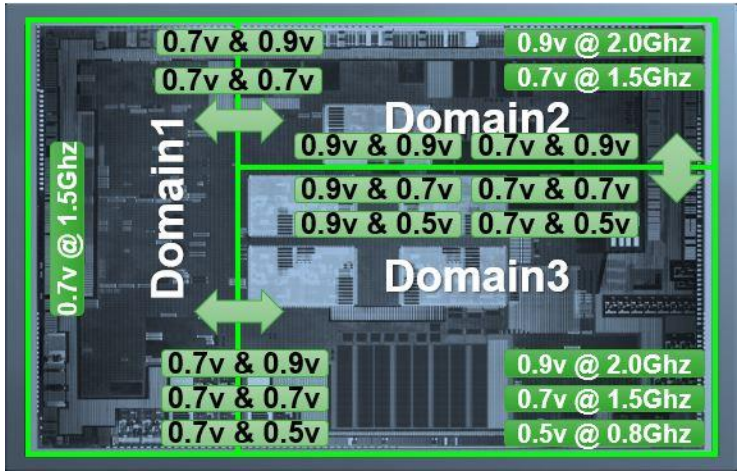
Where:

- $\sum_{i=0}^{m} \frac{p_i}{100} = 1$
- sg_0 represents the Single-Voltage logic, constituting a percentage p_0 of the design, with $n_0=1$
- XPO = cross domain path propagation overhead – generally very small

SMVA with DVFS STA compute resource estimation

Example

- For the multi domain design at slide 4
  - Assuming up to 5% paths crossing between Domain2 and Domain3



R = r*(0.3*1 + 0.3*2 + 0.4*3) + XPO = r*2.1 + XPO = r*2.19

XPO = r*0.05*0.3*6 = r*0.09

Domain	Domain size [% of total design logic] p	Voltage levels Count n
Domain1	30	1
Domain2	30	2
Domain3	40	3