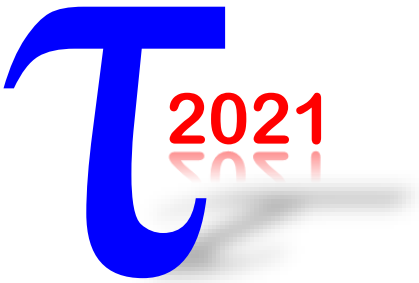

April 8th, 9th

Paul Pereira – General Chair

Jignesh Shah – Technical Program Chair

Tau 2021 Sponsors – Thank you!

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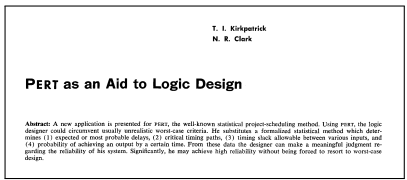
A Bit of History

Kirkpatrick, T. I., and N. R. Clark. "PERT as an aid to logic design." IBM journal of Research and Development 10.2 (1966): 135–141.



T. I. Kirkpatrick
N. R. Clark

PERT as an Aid to Logic Design

Abstract: A new application is presented for PERT, the well-known statistical project-scheduling method. Using PERT, the logic designer could circumvent usually unrealistic worst-case criteria. He substitutes a formalized statistical method which determines (1) expected or most probable delays, (2) critical timing paths, (3) timing slack allowable between various inputs, and (4) probability of achieving an output by a certain time. From these data the designer can make a meaningful judgment regarding the reliability of his system. Significantly, he may achieve high reliability without being forced to resort to worst-case design.

55 years of progress.

- STA provides
  - A probability distribution for slack
  - Critical paths
- Benefits of model
  - Relaxation over worst-case analysis
  - Handles skewed distributions
  - Handles correlation
- Limited by
  - Lack of good libraries
  - Lack of good variation models
  - Multi-input switching

Call for Support

- **Submit papers**
  - Tau is a workshop, both practical application and theoretical research work are welcome
  - You can still publish your paper at other conferences (DAC, ICCAD, DATE, ISLPED, ISQED, etc.)
- **Volunteer talks**
  - Share your perspectives and experiences
  - Both solutions and questions
  - Pose challenges and controversial topics
- **Establish a network**
  - Connect with academia, EDA, industry: challenges, ideas, collaborations, etc.
  - Academia/industry: please submit ideas/challenges and participate in the Tau contest!

Participation

- Approximately 50 attendees
- Academia, EDA, design houses, foundries
- Registrants as of last week:
  - Fraunhofer Institute, KTH Royal Institute of Technology, National Taiwan U., UC Santa Barbara, U. Illinois, U. Thessaly, U. Utah, Southeast University
  - Apple, Broadcom, DE Shaw Research, Global Foundries, Google, Huawei, IBM, Inphi, Intel, Liberty Software, Nordic Semi, Qualcomm, Rigoron, TSMC

Organization

Organizing Committee

- Paul Pereira (Qualcomm) - General chair
- Jignesh Shah (Intel) - Program committee chair
- João Geada (Ansys) - Past general chair

Contest Committee

- Walid Elgharbawy (Intel) - Contest Chair
- George Chen (Intel)
- Ted Hong (Google)
- Bogdan Tutuianu (TSMC)
- Anton Belov (Synopsys)

Technical Program Committee

- Jignesh Shah (Intel) - Program committee chair
- Satheesh Balasubramanian (ARM)
- Anton Belov (Synopsys)
- Mayur Bubna (Synopsys)
- Prasanjeet Das (Cadence)
- João Geada (Ansys) - Past general chair
- Masanori Hashimoto (Osaka University)
- Tsung-Wei Huang (University Of Utah)
- Oleg Levitsky (Intel)
- Kelvin Le (Google)
- Peivand Tehrani (Synopsy)
- Oscar Ou (Mediatek)
- K.S.Ramesh (Intel)
- Siddharth Sawant (Global Foundary)
- George Chen (Intel)
- Debjit Sinha (Google)
- Jeffrey Hemmett (IBM)
- Ken Stevens (University Of Utah)
- Walid Elgharbawy (Intel)

2021 Program Highlights

- **Keynotes and Invited Talks**
  - *ASTA for Cyclic and Asynchronous Circuits*, Christos Sotiriou (University of Thessaly)
  - *Simultaneous Multi Voltage Analysis with Dynamic Voltage Frequency Scaling*, Paul Berevoescu (Synopsys)
  - *Robust Rare Circuit Failure Detection using Data-Efficient Machine Learning*, Peng Li (University of California, Santa Barbara)
  - *The OpenROAD Project : Goals, Demo, and Code Organization*, Tom Spyrou (University of California, San Diego)
  - *Use of AI/ML in Engineering Simulation*, Prith Banerjee (Ansys)
  - *Aging Timing Signoff Solutions for Automotive and IoT Applications*, Siddharth Sawant (Global Foundries)
  - *Efficient Parasitic Interconnect Insertion for Timing Analysis*, Ron A. Rohrer (Southern Methodist University)
  - *The Evolution, Pitfalls, and Cargo Cult Engineering of Advanced Digital Timing Sign-off*, Christian Lutkemeyer (Inphi)
- **Panel**: How many sigmas are enough?
- **Contest**: CCS delay calculation

Logistics

- **Proceedings**
  - Papers are available now via the chat window.
  - Proceedings with most workshop presentations will be distributed after workshop through the Cvent registration list.
- **Hours**
  - Main sessions are from 8:00 am to 4:00 pm (PST)
  - Zoom conference is open from 7:00 am to 7:00 pm (PST)
- **Breaks and Lunch**
  - No catered meals, unfortunately.
  - Will randomly assign to breakout rooms, feel free to arrange side meetings through private chat.
- **Presenters**
  - Please email slides to jignesh.shah@intel.com, paulpere@qti.qualcomm.com if you have not done so as a backup.