Accurate Gate Delay Model for Arbitrary Waveform Shapes

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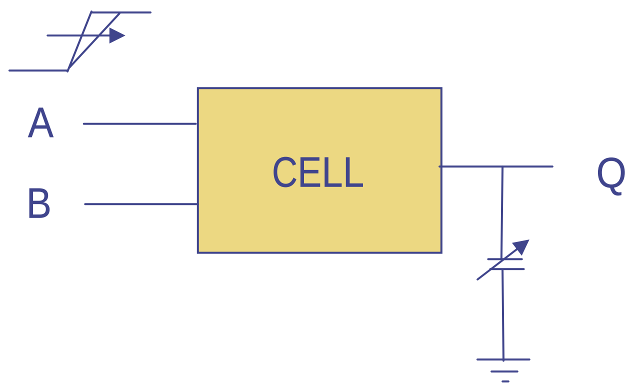
Motivation

- **Static Timing Analyzers**
  - Used to verify behavior of large digital circuits
  - Core engine is circuit optimization tools
- **Current Timing Analyzer**
  - Cell Based Models
  - Fails to capture the shape of complex the waveform
- **Our Work**
  - Methods for accurate modeling of arbitrary gate input and output waveforms

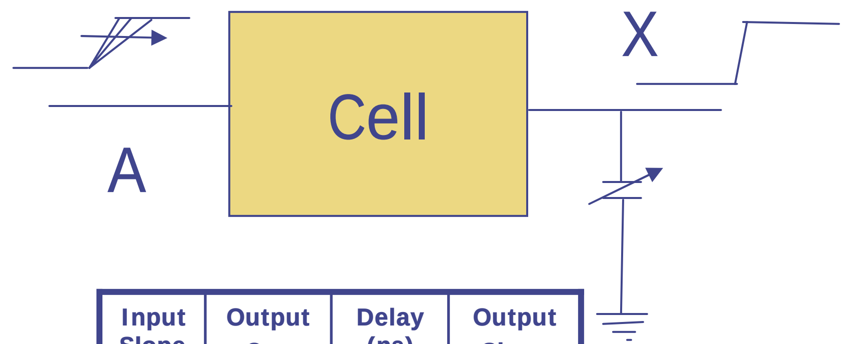


Outline

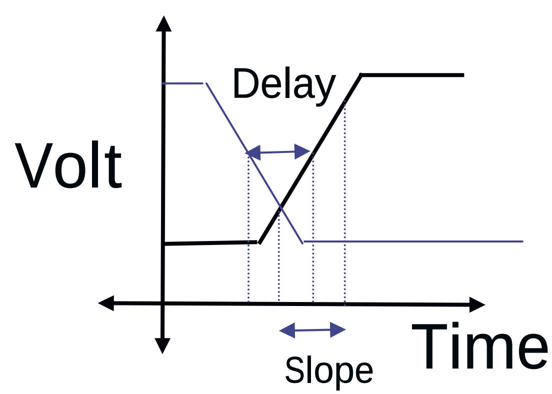
- **Motivation and Previous Work**
- Proposed Delay Modeling
- Base Waveform Selection Method
- Results
- Conclusion

Cell Based Approach

- **Traditional Gate Delay Model**
  - 2-D characterization tables for 20%-80% output slew and 50% output delay
- **Advantages**
  - Simple and fast runtime
- **Disadvantages**
  - Characterization effort. (2-D input characterization space with multiple process corners)
  - Accuracy is a concern as we fail to capture the shape of complex waveforms



Input Slope (ns)	Output Cap	Delay (ns)	Output Slope (ns)
.2	2fF	.23	.15
.25	2fF	.28	.22
.2	4fF	.31	.19
.25	4fF	.35	.27



Waveform Approximation

Ramp Approximation

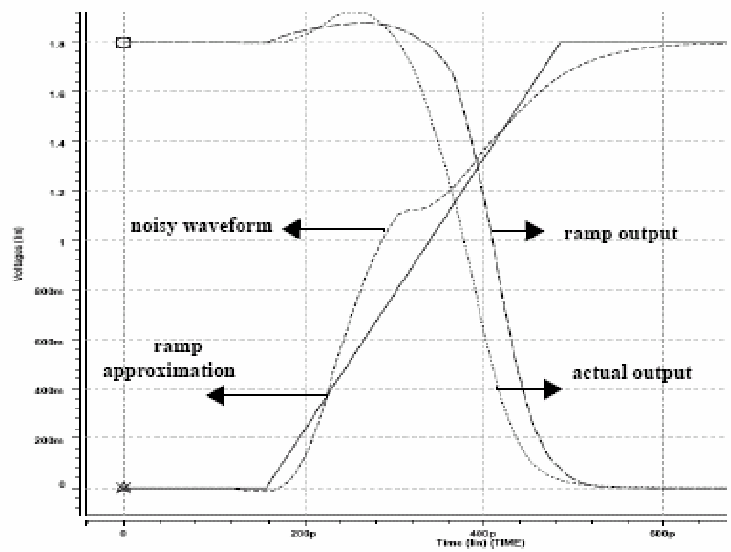
- Significant inaccuracy for non ramp signals.
- Worsens with as technology scales.

Occurrences of Non-Ramp signals

- Capacitive coupled nodes
- Long routes with considerable inductance (ringing)
- Resistive shielding
- Mutual inductance
- Supply noise

Challenges

- General method applicable to wide range of waveform shapes
- Maintain simplicity and efficiency of traditional model



Other Proposed Approaches

- M. Hashimoto, Y. Yamada, H. Onodera, *"Equivalent Waveform Propagation For Static Timing Analysis",* ICCAD 2003
  - Fitting for input waveforms using ramp using least quares
  - Output waveform not considered
- C. Amin, F. Dartu, Y. Ismail, *"Weibull Based Waveform Model",*ICCAD 2003
  - Good match for monotone signals
  - Characterization Space increased with 3rd parameter
- S. Nassif, E. Acar, *"Advanced Waveform Models for the Nanometer Regime",* TAU 2004
  - Interesting approach but does not discuss the application of the approach with respect to gate delay model and timing analysis

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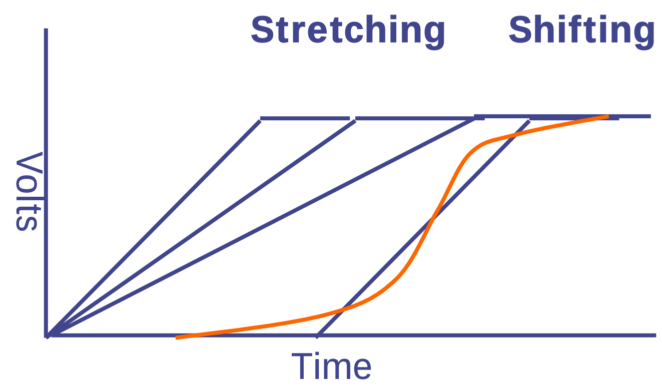
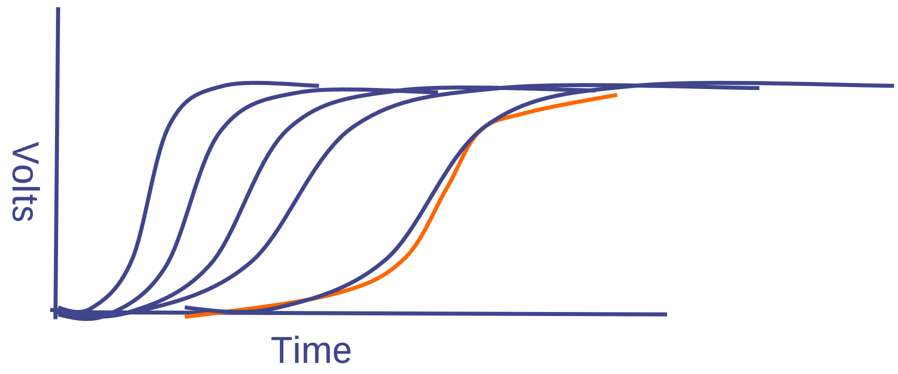
Stretching and Shifting Waveform

- Traditional Fitting Approach
  - Slope = Stretch Factor
  - Adding delays in STA = Shifting Waveform
  - Fitting Crossing times and 20% and Objective is to match 50% Vdd 80% Vdd Transition time
  - Ramp Shape Assumed
- Proposed Fitting Approach
  - Stretch and shift arbitrary shape waveform
  - Minimize the weighted least square difference

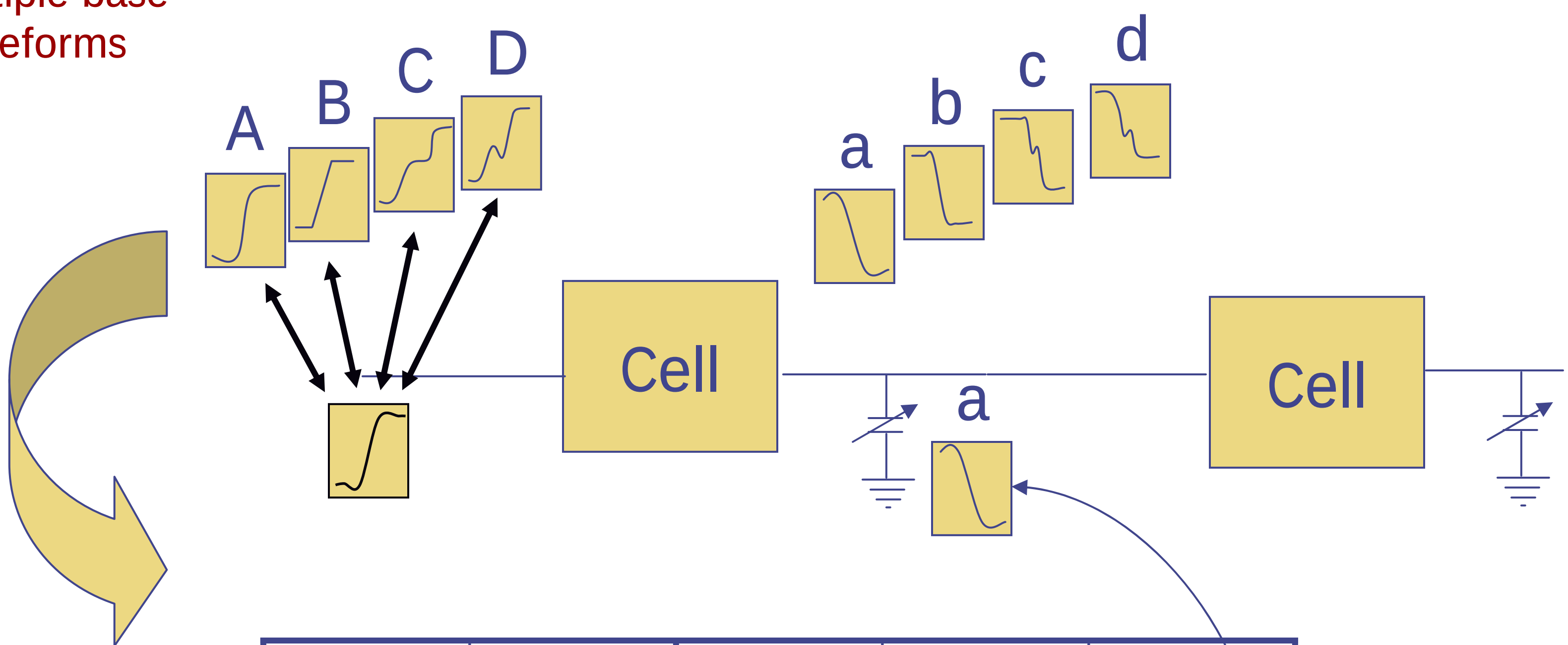
    (Considers entire waveform)
  - Using multiple waveforms to model arbitrary waveform shapes





Proposed Timing Analysis

- Multiple base waveforms



- Evaluating fit of each base waveform using shift and stretch
- Selection of the best base Waveform.

Stretching Factor	Output Cap	Output Wave	Stretching Factor	Shifting Factor
.85	**2fF**	**a**	**1.23**	**-20.8**
.95	2fF	b	1.10	-30.2
1	2fF	a	1.3	-24.6

Closure Property

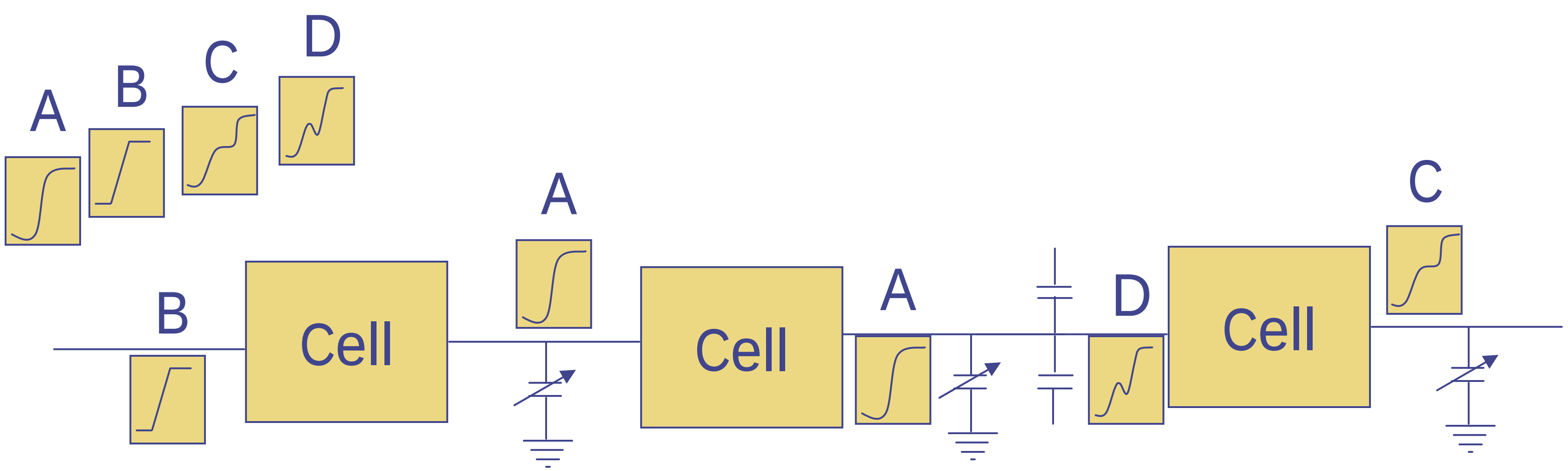
- Use the same set of base waveforms for input and output waveform modeling

For Local Interconnects

- New waveform is not constructed but shift and stretch factors along with the base waveform type are directly propagated
- Fast, and runtime comparable to traditional STA

For Global Interconnects

- Shape of the waveform changes due to interconnect and hence new waveform must be re-fitted
- Accuracy much better than traditional STA



Proposed Representation of a Waveform

- Proposed Waveform Representation
  - Specifying a waveform as vector of n time points

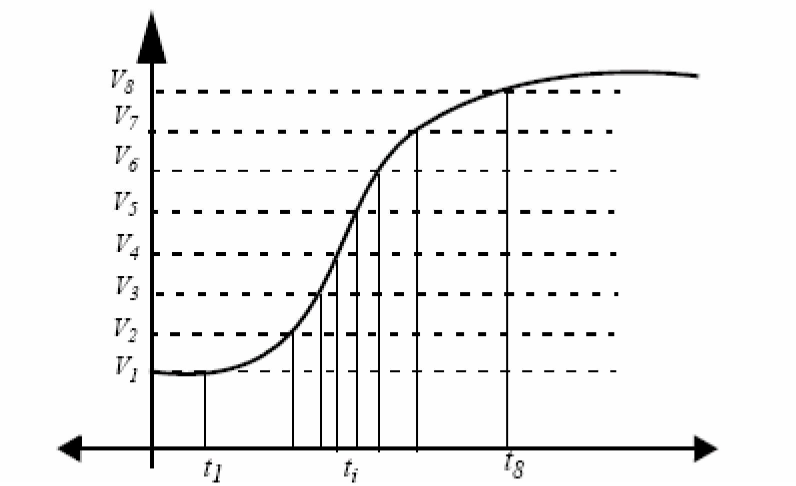
    $[T] = \{ t_1, t_2, t_3, t_4, t_5, \ldots\ldots\ t_n \}$

    where t_i is the time that the waveform crosses voltage $i\,(V_{dd}/n)$

  - $[R] = t_a + s.[T]$ where

    s = Stretching factor

    t_a = Shifting



Which set of base waveforms is best to use in timing analysis?

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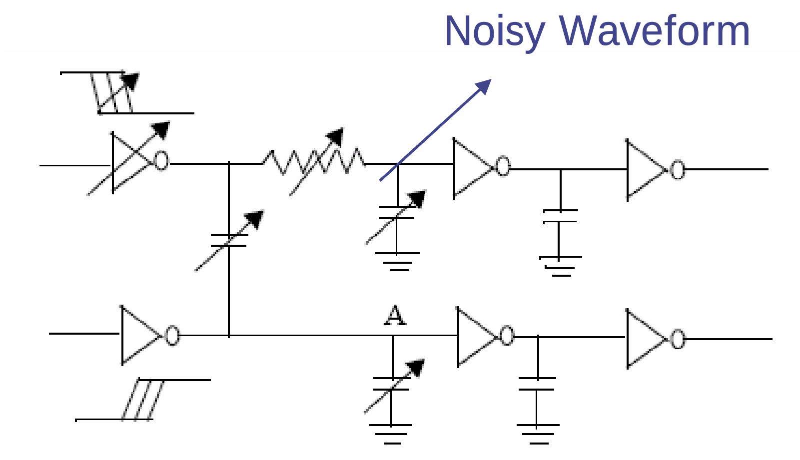
Proposed Methodology

- **Proposed Methodology (Objectives)**
  - Minimum number of base waveforms for given error threshold
  - Select arbitrary number of base waveforms depending upon desired accuracy

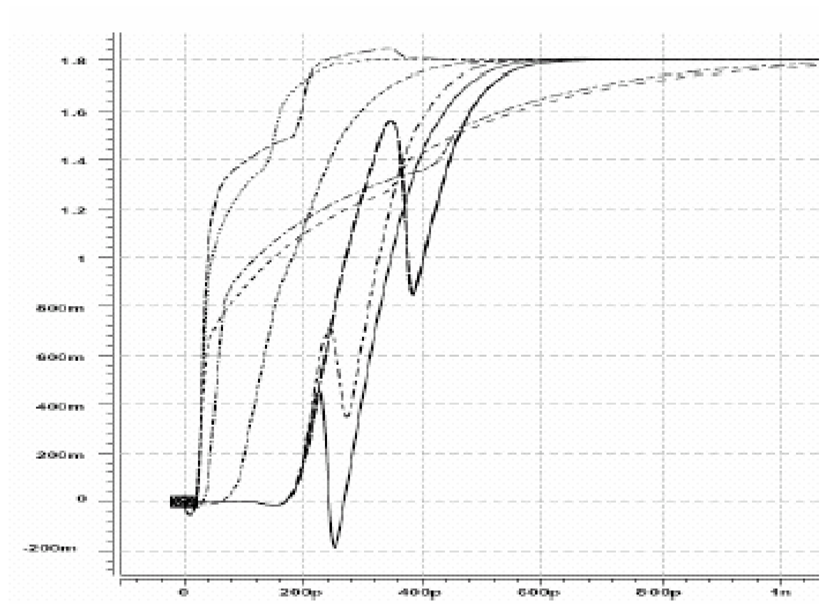
- Under closure optimal Selection of Base Waveforms maps to a 3D covering problem which is infeasible

- **Proposed Simplified Method**
  - **Construct set of input base waveforms**
    - Generate large set of *candidate waveforms*
    - Use candidate waveforms as possible base waveforms
    - Generate an error matrix
    - Generate cover matrix
    - Solve the covering problem to select required base waveforms
  - **Select output base waveforms from input base waveforms**

Generating Candidate Waveforms



- **Generation of Candidate Waveform (*Wc*)**
  - Base Waveforms (*Wb*) are selected from Candidate Waveform
  - Capacitively coupled nodes' Waveforms
  - Inductive Ringing Waveforms
  - Mutually Inductive Waveforms

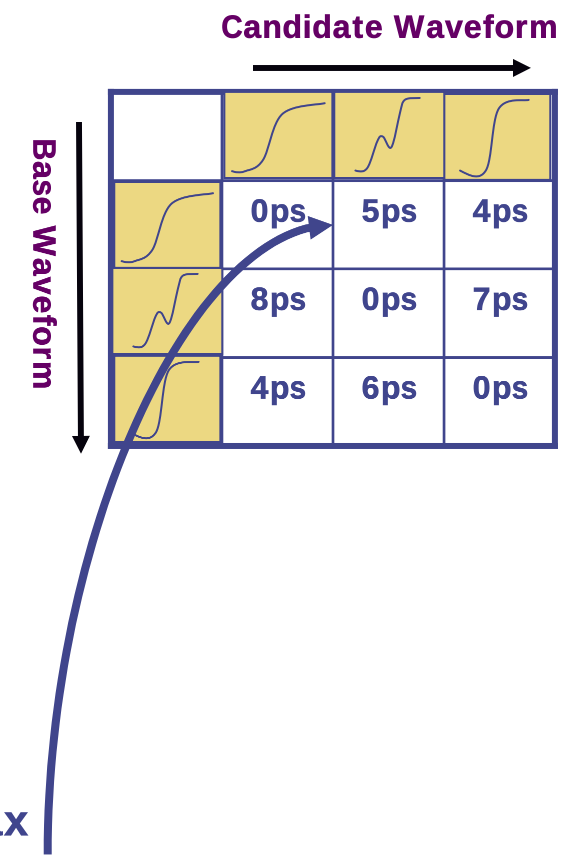


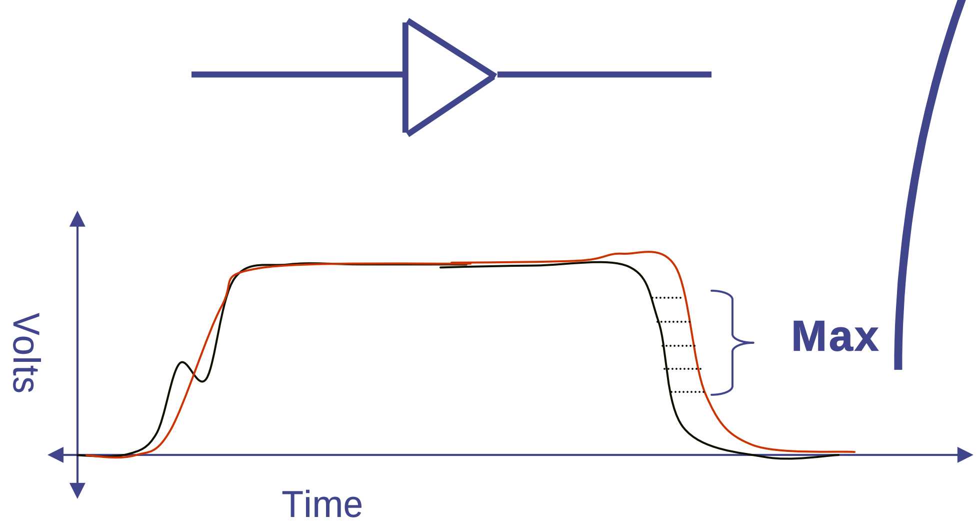
Generation of Error Matrix

- **[H] = r + s x [T]**

  Any waveform [H] can be represented as shifted and stretched version of a base waveform.

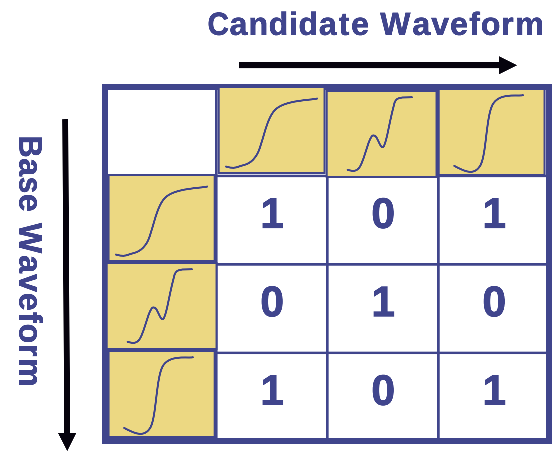
- *n** (*n-1*) spice simulation where n is the number of candidate waveform waveform





Generation of Cover Matrix.

- Threshold ε
- If C(i,j) = 0 if E(i,j) > $\varepsilon (= 4)$
  else C(i,j) = 1



Cover Matrix

- Unate Covering Problem
- Select a set of rows such that each column has at least one “1” in a selected row
- Solving the Unate Covering Problem gives us the base waveform set
  - Efficient heuristics available

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Results

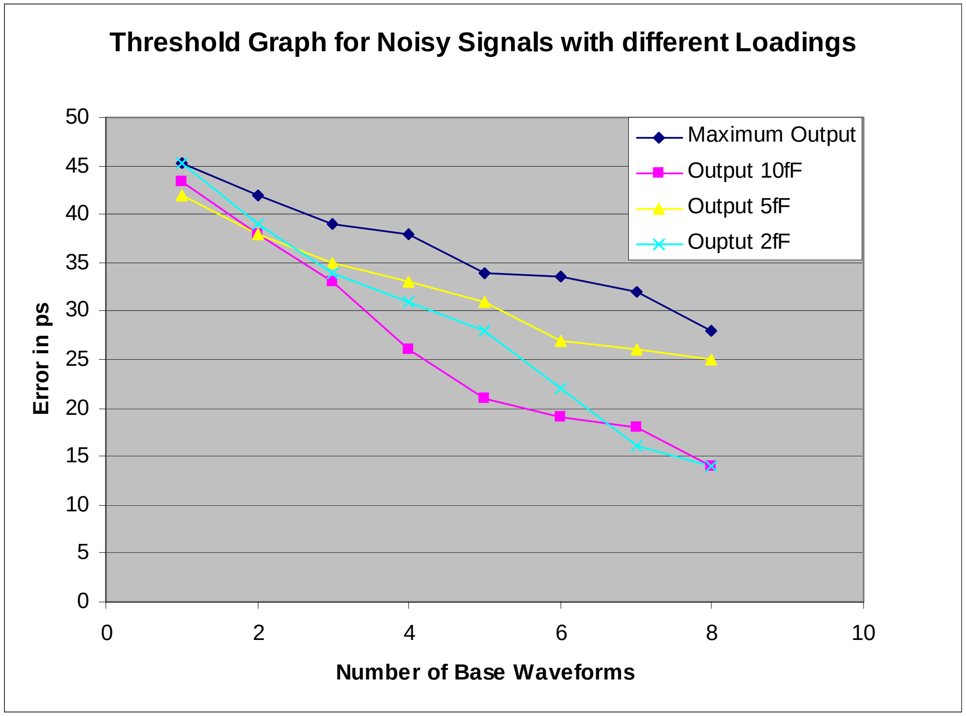
Output Capacitance	Ramp Waveform		Proposed Approach		
	Least Square Methods	10%-90% Fitted	Single Waveform	Two Waveform	Five Waveform
10fF	64.4ps	93.3ps	43.3ps	38ps	21ps
5fF	59.3ps	91.6ps	42.0ps	37.5ps	31ps
2fF	64.4ps	90.6ps	44.6ps	37ps	28ps
Maximum Matrix	64.4ps	93.3ps	44.6ps	38ps	34ps

Decrement of error from 93.3ps to 44.6ps without increasing characterization space

Comparison between Proposed and Traditional Approaches

- These experiments were done with 381 candidate waveforms out of which 200 were capacitively coupled, 179 inductive ringing and 2 were mutually inductive noisy waveform

Threshold Graph for the Input Waveform



Threshold Graph for Different Loading for input noisy waveforms

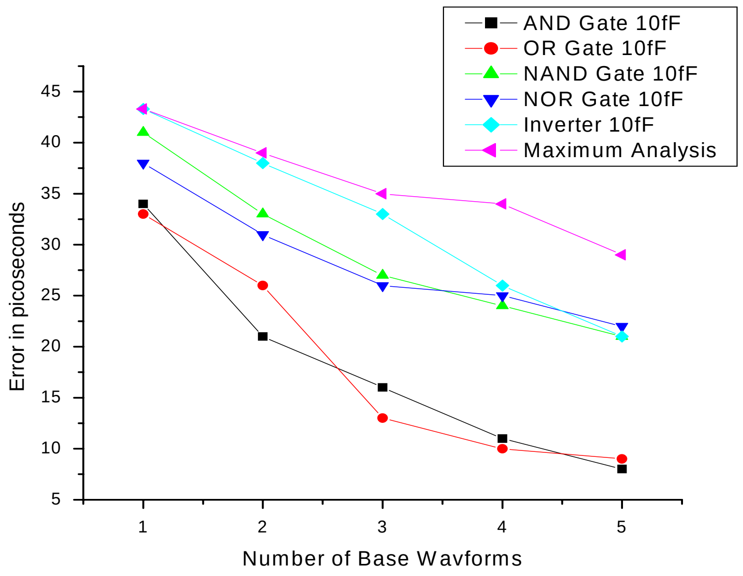
- As the Maximum allowable error increases the number of waveforms decreases

Comparison Across Library Cells

Gate Type	Ramp Waveforms		Proposed Waveforms		
	10%-90% Fitted (ps)	Linear Fitted (ps)	Single Waveform (ps)	Two Waveform (ps)	Five Waveform (ps)
NAND	85.1	59.8	41	33	22
NOR	79.8	57.2	37.9	31	23
AND	108.2	56.7	33.9	21	7
OR	106.6	55.9	33	27	8
Inverter	93.3	64.4	43.3	38	21
Maximum	106.6	64.4	43.3	39	34

- Comparison between the traditional approach and proposed approach for different gates from a library with a constant output loading

Threshold Graph Across Library Cells

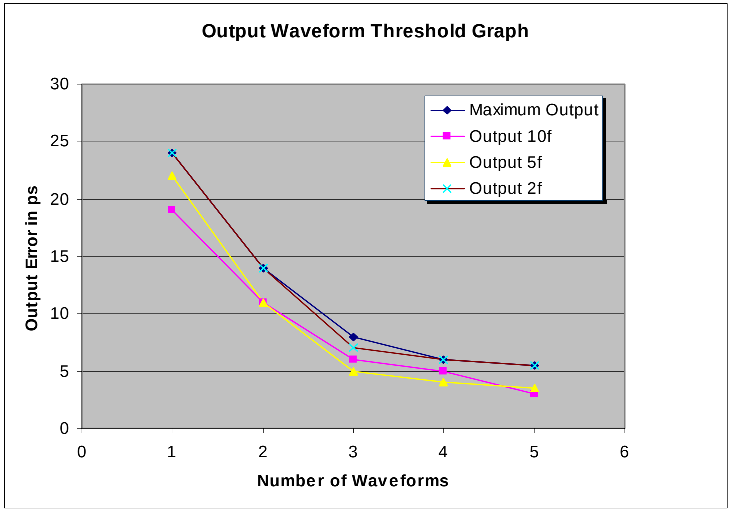


Threshold Graph combining all types of Gates

Error and Threshold Graph for Output Waveforms

Gate	One Waveform	Two Waveform	Five Waveform
And	20.3ps	13.4ps	9.1ps
OR	21.4ps	13.7ps	8.9ps
NOR	21.1ps	14.1ps	9.4ps
NAND	22.3ps	13.9ps	9.2ps
Inverter	25.1ps	15.2ps	9.7ps
Max. Across Gates	25.8ps	15.5ps	10.1ps

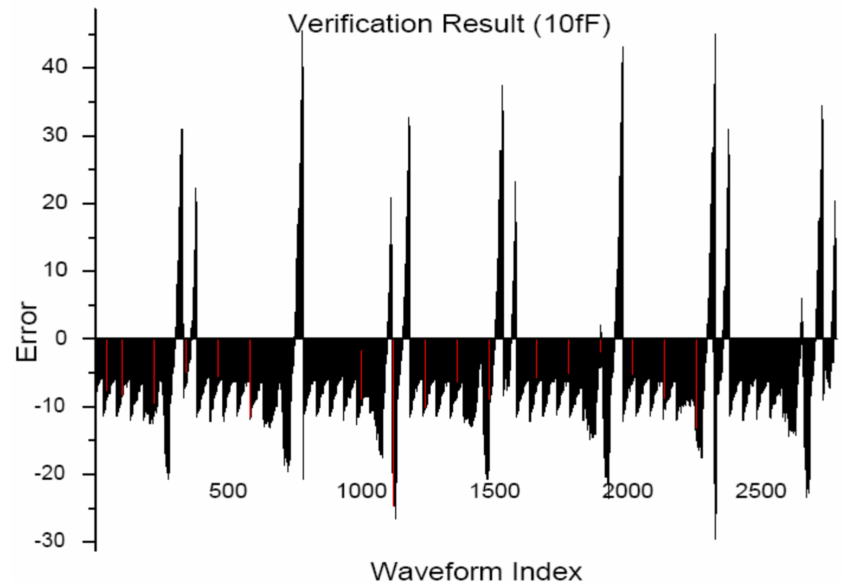
Error Waveform at Output with Closure



Threshold Graph

Verification

- Verification Results
  - 2781 Waveforms generated to test the accuracy of the proposed gate delay model
  - A single base waveform was used
  - Maximum error predicted using the approach was 43.4ps
  - Actual maximum error using the test waveforms with spice was 44.4ps
  - The introduced error of about a Pico-second is attributed to the interpolation error



Conclusion

- In this work we have proposed a new methodology for gate delay model for arbitrary waveform shapes that traditionally were difficult to model with simple ramp approximation without exponentially increasing input characterization space
- Using this approach the maximum error decreases from 93.3ps to 43.3ps by selecting only a single base waveform
- This cost of fitting is generally much less than that of signal convolution used for inter-connect simulation
- Also, the cost of selecting the base waveform is amortized for the entire library and is a one-time cost

- Questions?