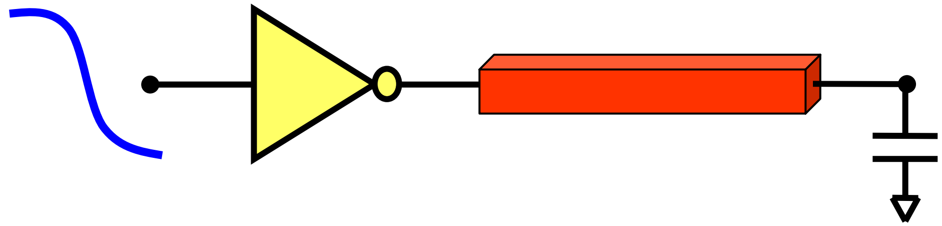

Statistical Static Timing Analysis: How simple can we get?

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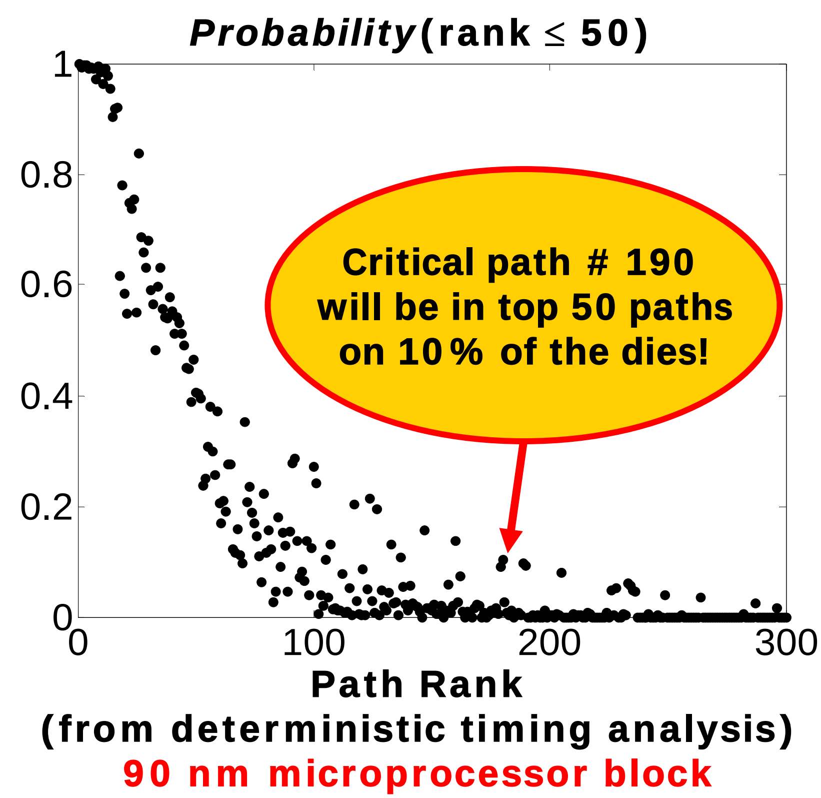
Outline

- Introduction
- Process Variation Model
  - Distributions
  - Cell-library characterization
- Methodology
  - Path-based
  - Add/Max Operations
- Results
- Conclusions

Variations and their impact

- Sources of Timing Variations
  - Channel Length
  - Dopant Atom Count
  - Oxide Thickness
  - Dielectric Thickness
  - Vcc
  - Temperature
- Influence
  - Performance yield prediction
  - Optimization
  - Design convergence
- Management (traditional)
  - 'Corner' based analysis
    - Sub-optimum



Recent solutions

- Categories
  - Block-based pdf propagation
    - Non-incremental
    - Incremental
  - Path-based pdf propagation
  - Bound calculation
  - Generic path analysis
- Complexity
  - Non-gaussian pdf propagation
  - Statistical MAX operation
  - Correlations
  - Reconvergence

Factors influencing solutions

- Predicting performance yield or optimizing circuit?
- Underlying process characteristics
  - How significant are the variation sources?
  - How significant is each component?
    - Die-to-die / Within-die
    - Channel length, Threshold voltage, etc
- Architecuture and Layout
  - Number of stages between flip-flops
  - Spatial arrangement of gates

SSTA targets

- Performance yield optimization
  - Die-to-die effects are more important
  - Can be handled using a different methodology
- Design convergence
  - Affected primarily by within-die effects
  - Gate’s delay w.r.t. others’ on the same die

Presented work addresses **design convergence**

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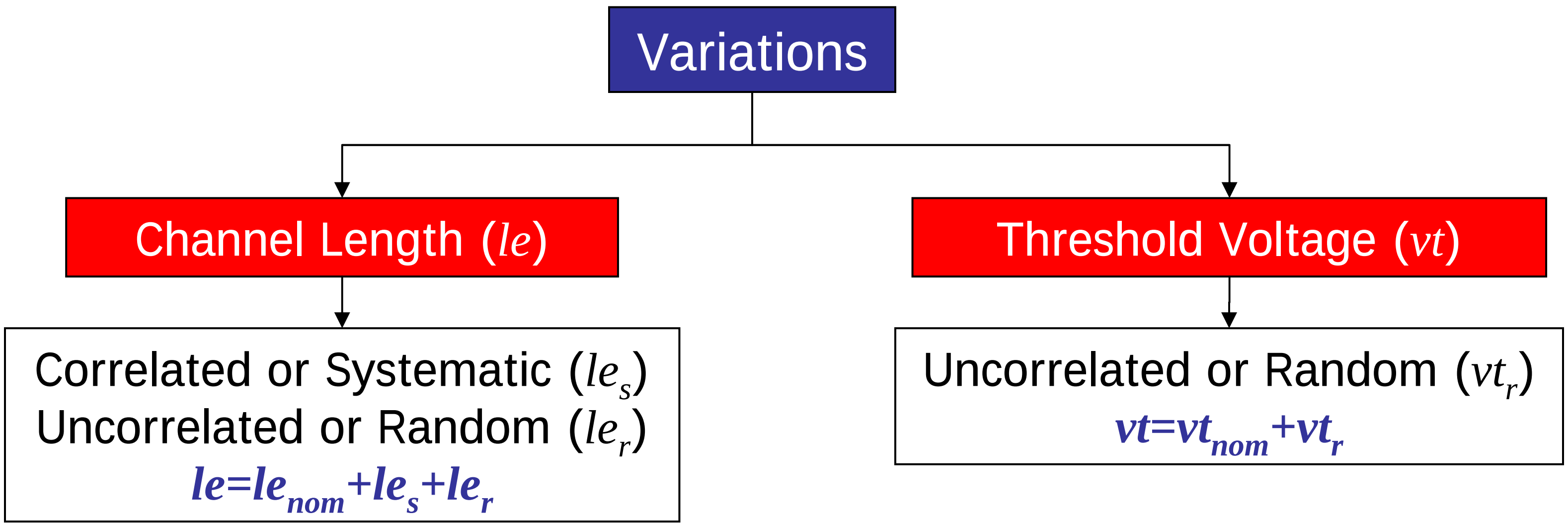
Modeling variations

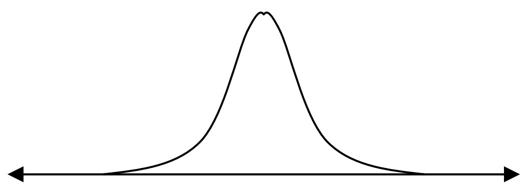
- Only within-die effects considered



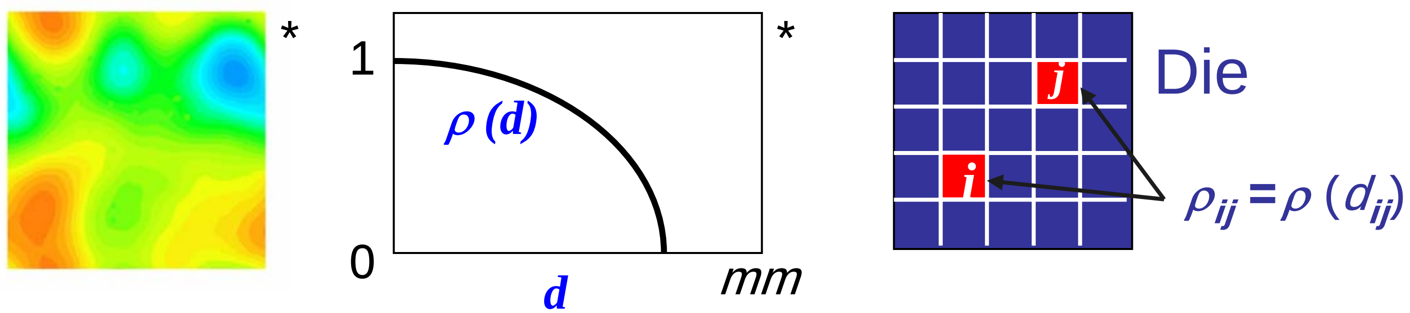
Main variations affecting delay: *le* and *vt*

Parameter distributions

- Gaussian distributions for le_s, le_r, vt_r
  - Characterized by σ_{les}, σ_{ler}, σ_{vtr}



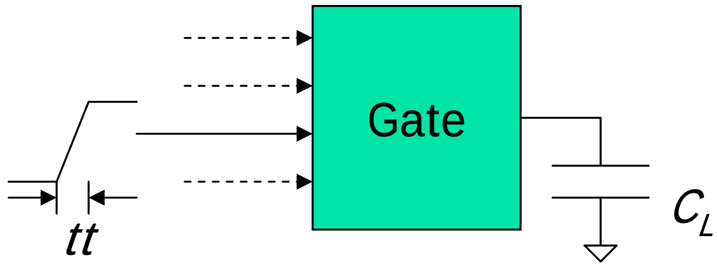
- Systematic variation for le_s
  - Correlation is a function of distance



*[16] S. Samaan, ICCAD ‘04

Cell-library characterization

- Simulations similar as for deterministic STA
  - Plus extra simulations for measuring Δdelay



$$delay = delay_{nom}(le_{nom}, tt, C_L)$$

$$+ \Delta\, delay_{les}(le_s, tt, C_L) + \Delta\, delay_{ler}(le_r, tt, C_L) + \Delta\, delay_{vtr}(vt_r, tt, C_L)$$

effects of variations on delay

$$\sigma^2_{delay} = \sigma^2_{delay,les}(\sigma^2_{les}, tt, C_L) + \sigma^2_{delay,ler}(\sigma^2_{ler}, tt, C_L) + \sigma^2_{delay,vtr}(\sigma^2_{vtr}, tt, C_L)$$

Overall delay variance is the sum of variances due to le_s, le_r, and vt_r

Measuring σ_{delay}

- Characterization of $\sigma_{delay,les}$
  - Vary le similarly for all transistors in the cell (ρ=1)
  - Measure delay change for each input to output arc
- Characterization of $\sigma_{delay,ler}$ and $\sigma_{delay,vtr}$
  - Sample using Monte Carlo method
    - Each transistor sampled independently
  - Measure delay change for each input to output arc

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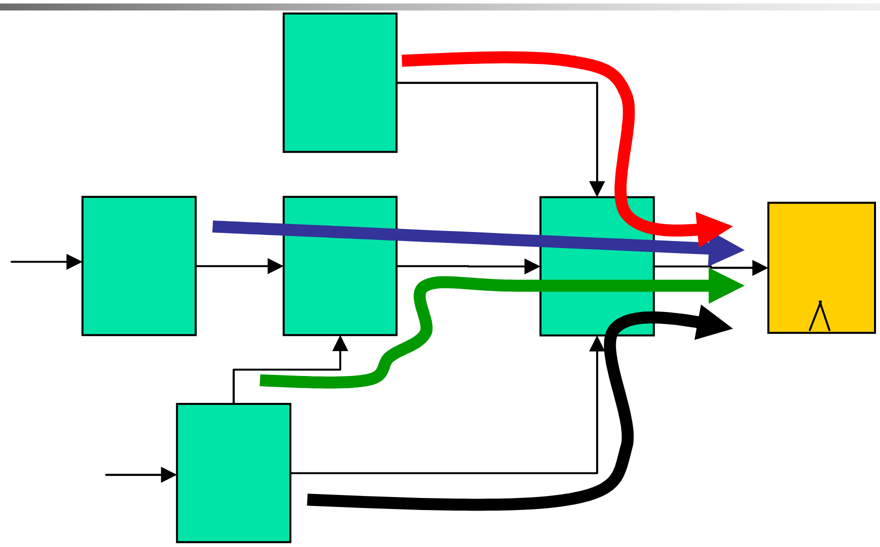
Variation effects on a path

- Systematic variations
  - Additive effect
    - $(\sigma/\mu)_{path\text{-}delay} = (\sigma/\mu)_{cell\text{-}delay}$
  - Spatial effect
    - Paths close together have very similar delay variation
- Random variations
  - Cancellation effect
    - Variations die out as long as there are enough stages
    - $(\sigma/\mu)_{path\text{-}delay} = (1/\mathrm{sqrt}(n))*(\sigma/\mu)_{cell\text{-}delay}$
    - ITRS projections: n~12 stages

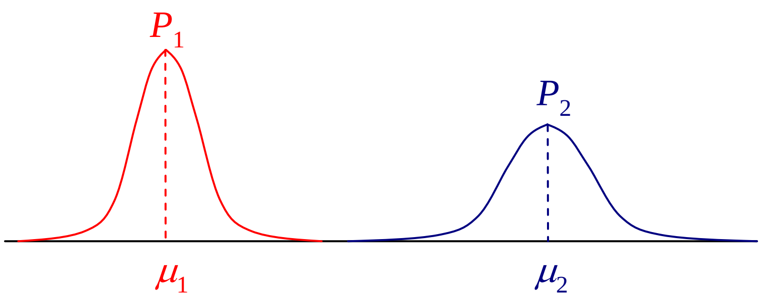
Paths converging on a flip-flop



- Distribution of delay for each path known
  - From simple path-based analysis
- Distribution of overall margin at flip-flop?
  - Statistical MAX operation!

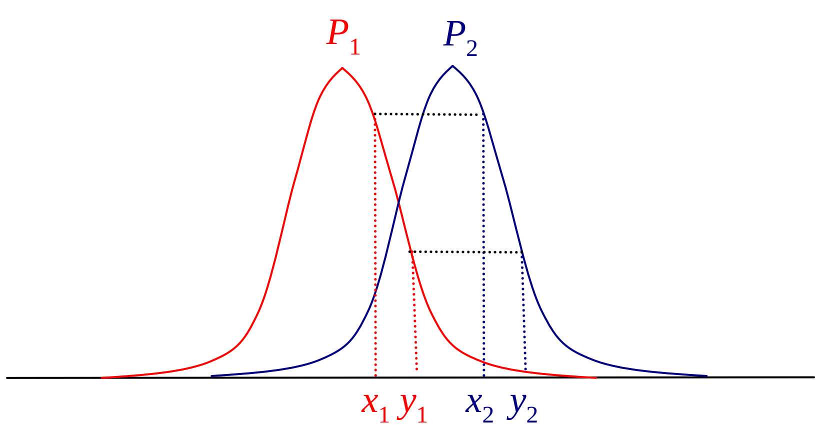
Statistical MAX operation

1 **Non-overlapping**

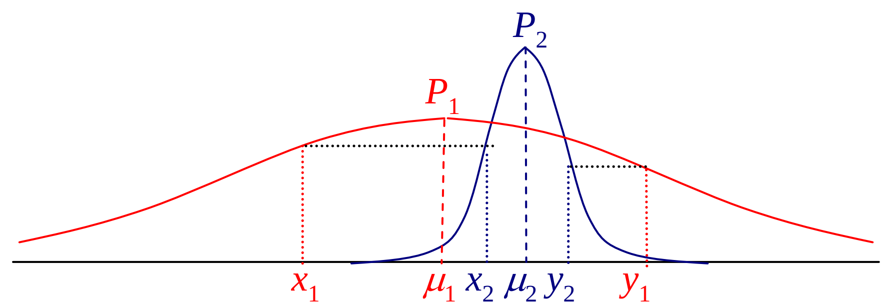


**MAX is trivial,
and situations observed on circuits**

2 **Highly correlated, overlapping, comparable sigmas**

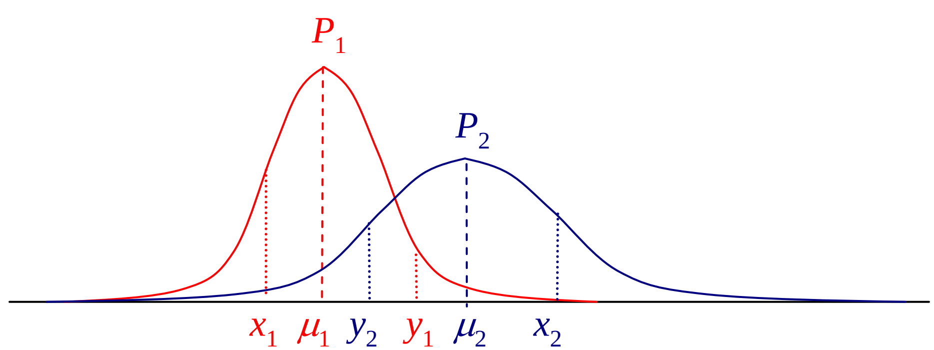


3 **Highly correlated, overlapping, different sigmas**

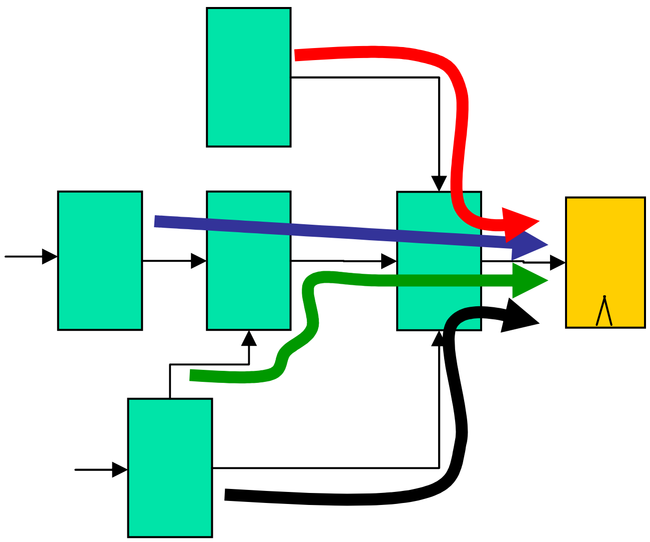


**MAX is non-trivial, but
situations not observed on circuits**

4 **Random, overlapping**



Comments about MAX



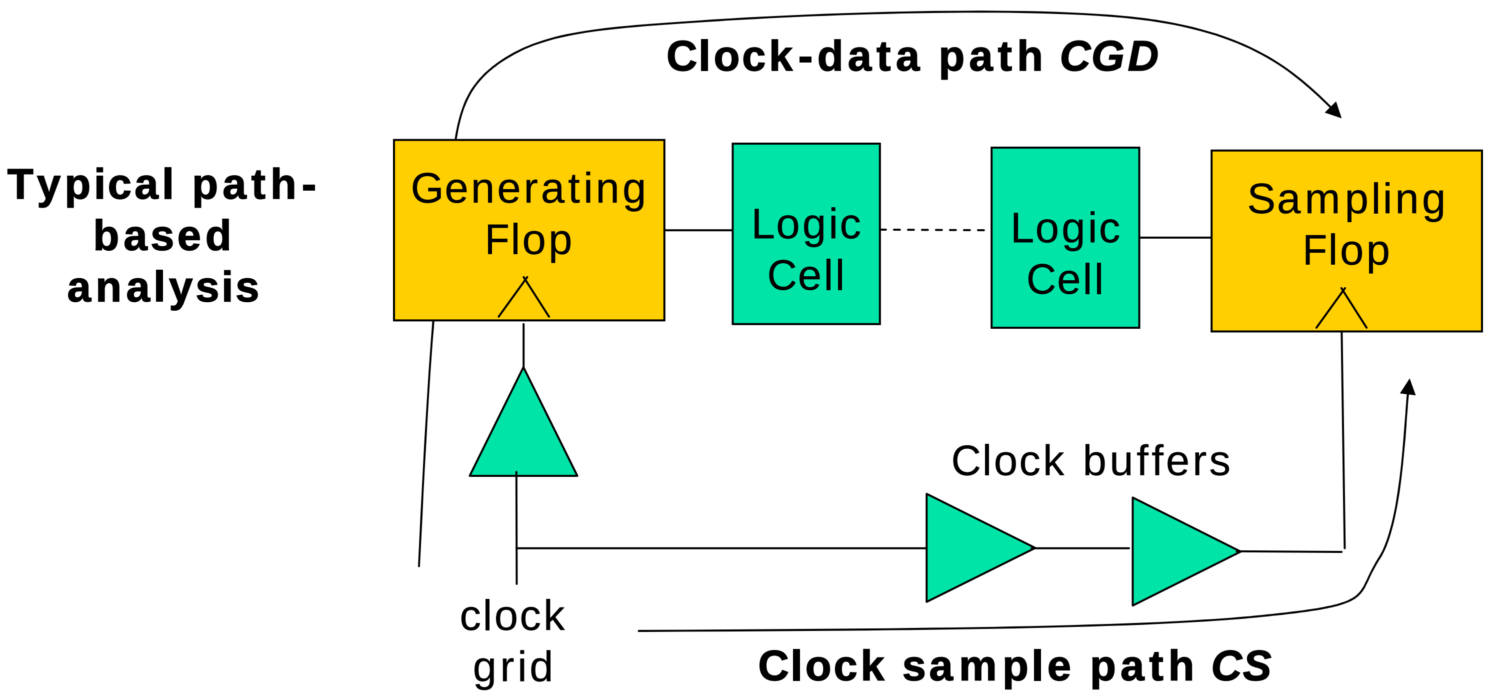
- Path-delays are highly correlated
- Sigmas are similar
- Random components die out due to depth

No need for a complicated MAX operation!!

Path-based SSTA methodology

Main Idea

Calculate the timing-margin distribution, for each path ending at a flip-flop or a primary output (PO)

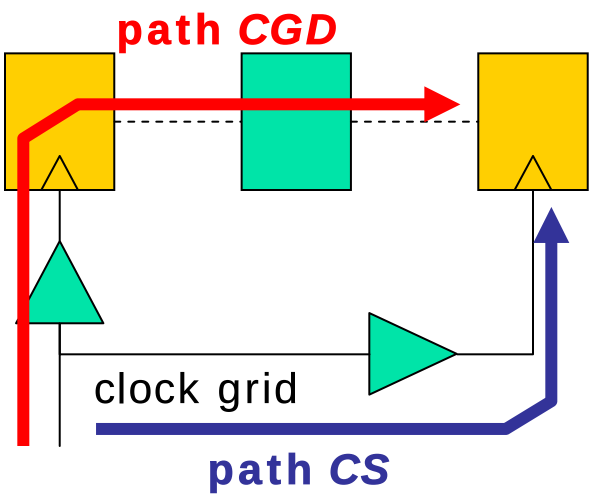


Calculating margin distribution

$$margin = t_{cs} + T - t^{*}_{CGD}$$

*includes t_{setup}

$$\sigma^2_{margin} = \sigma^2_{CS} + \sigma^2_{CGD} - 2 \cdot cov(t_{CS}, t_{CGD})$$



- σ_{CS} – delay sigma for path CS
- σ_{CGD} – delay sigma for path CGD
- $cov(t_{CS}, t_{CGD})$ – covariance between delays of CS and CGD

Above analysis requires calculating delay variances and covariances for paths → Statistical ADD operation

Statistical ADD

- Path delay variance is the sum of delay variances due to le_s, le_r, and vt_r

$$\sigma^2_{path\text{-}delay} = \sigma^2_{path\text{-}delay,les} + \sigma^2_{path\text{-}delay,ler} + \sigma^2_{path\text{-}delay,vtr}$$

Uncorrelated or Random Components

$$\sigma^2_{path-delay,ler} = \sum_{i=1}^{n} \sigma^2_{i,ler}$$

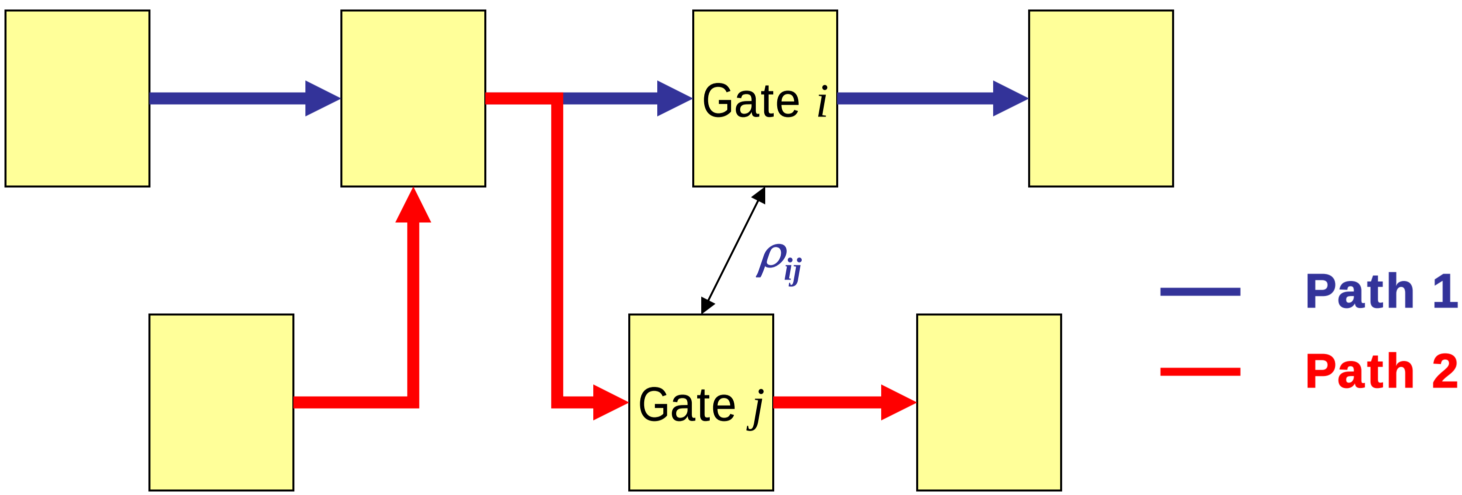
$$\sigma^2_{path-delay,vtr} = \sum_{i=1}^{n} \sigma^2_{i,vtr}$$

Correlated or Systematic Component

$$\sigma^2_{path-delay,les} = \sum_{i=1}^{n} \sigma^2_{i,les} \sum_{j=1}^{n} \rho_{ij} \sigma^2_{j,les}$$

Path-delay covariance

- Easy to calculate based on pair-wise covariances between individual gates



$$\sigma_{p1,p2} = \sum_{i \in p1} \sum_{j \in p2} \mathrm{cov}(cell_i, cell_j) = \sum_{i \in p1} \sum_{j \in p2} \rho_{ij} \sigma_{les,i} \sigma_{les,j}$$

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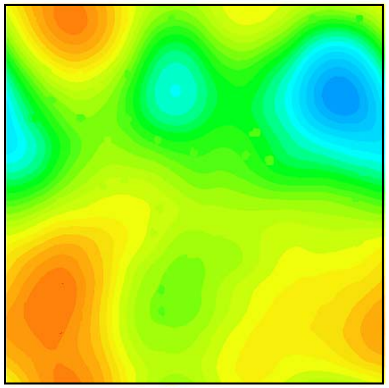
Results

- Methodology applied to a large microprocessor block
  - More than 100K cells
  - 90 nm technology
  - Fully extracted parasitics
- Block-based (BFS) analysis to identify top *N* critical end-nodes (flop inputs, POs)
- Critical paths identified by back-tracking
- Path-based SSTA performed on the critical paths
- Comparison with Monte Carlo Analysis

Monte Carlo

- 600 dies (profiles) for varying le_s, le_r, and vt_r
  - Number depends on correlation distance, block size, etc
- Full block-based analysis (BFS)
  - Not just on critical paths
  - Deterministic STA on each of the generated 600 dies

le_s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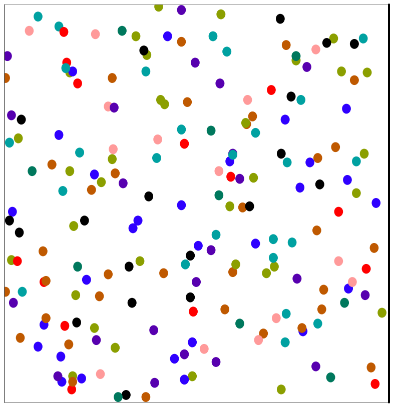
le_r and vt_r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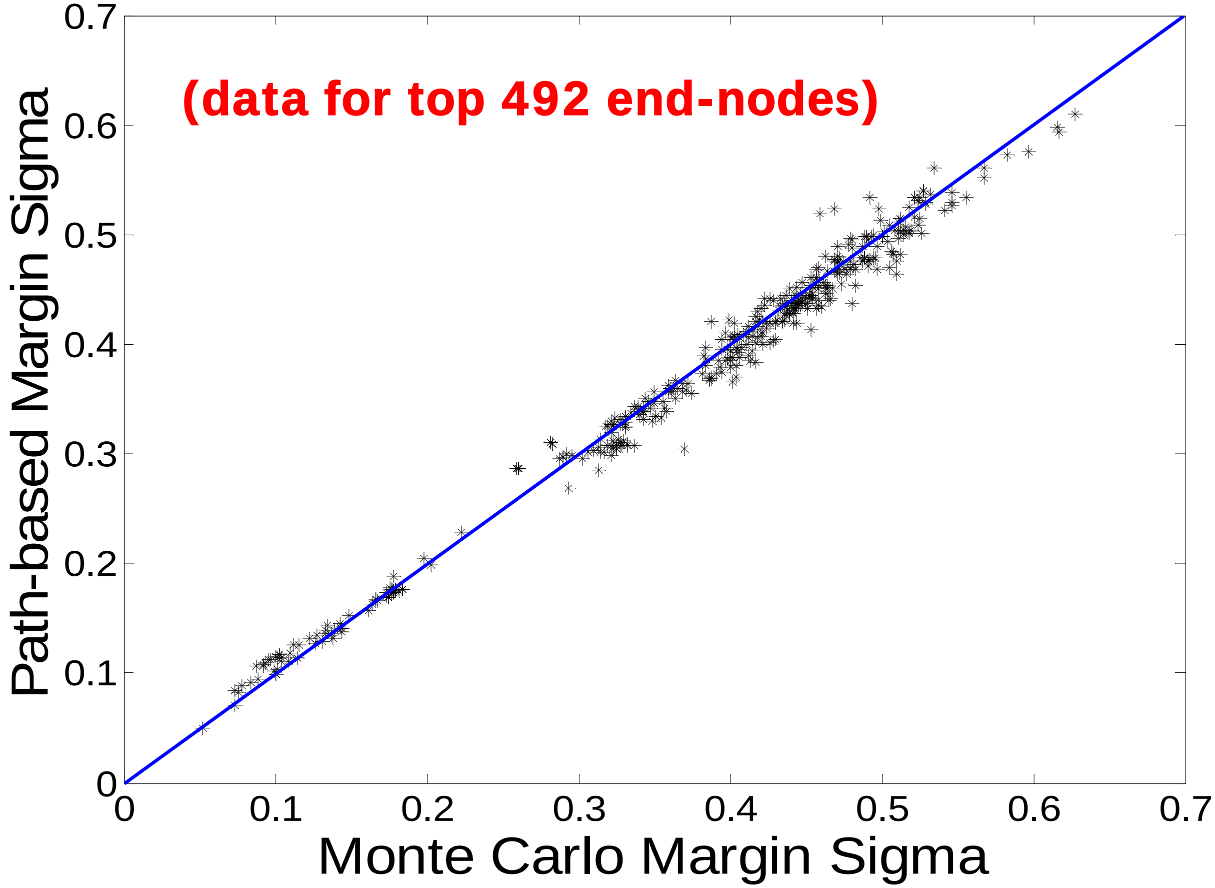
Comparison with Monte Carlo



Good correlation with Monte Carlo Results!

Analysis

- Error in predicting sigma
  - Maximum: 0.066 FO4 delay
  - Average: 0.19% of the path delay
- Monte Carlo showed that distributions of margins are Gaussian
  - No need for more complex distributions
  - At each end-node
    - Only one or two paths were clearly showing up as worst paths on 80% of Monte Carlo samples
    - Relative ordering of paths ending up at a node does not change

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Conclusions

- Statistical timing is important
- Simple path-based algorithm is adequate
  - Justified based on design, variation profiles
- Distributions are Gaussian
- Errors in estimating sigma are acceptable

Q & A