ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems

February 26-27, 2007

Preliminary Program

Day 1 (February 26, 2007)

Time	Event
8:00 – 8:30am	Registration / Breakfast
	Session 1: SSTA-I
8:30 – 10:10 am	Efficient Computation of the Exact Worst-Delay Corner Luis Guerra e Silva, Joel R. Phillips and L. Miguel Silveira Early Statistical Timing Analysis with Unknown Within-Die Correlations Khaled Heloue and Farid Najm Correlation-based Testing Path Selection under Process Variations using Statistical Timing Analysis Charlie Chen
	Criticality Aware Latin Hypercube Sampling for Efficient Statistical Timing Analysis Vineeth Thazhathu Veetil, David Blaauw and Dennis Sylvester
10:10 - 10:30am	Break
10:30am -12:10	Session 2: Statistical and Conventional Circuit Optimization
	Comparative Analysis of Conventional and Statistical Design Techniques Steven Burns, Keith Bowman, Noel Menezes, Mahesh Ketkar, Vivek De and James Tschanz Statistical Leakage Power Minimization Using Fast Equi-Slack Shell Based Optimization Xiaoji Ye, Yaping Zhan and Peng Li Fast Min-Cost Buffer Insertion under Process Variations Ruiming Chen and Hai Zhou Gate Sizing For Cell Library-Based Designs Shiyan Hu, Mahesh Ketkar and Jiang Hu
12:10pm- 1:30pm	Lunch
1:30-3:00 pm	Special Session 3: Electrical DFM Innovation: Communicating Variations to Designers Mustafa Celik (ExtremeDA), Andrew Kahng (BlazeDFM, UCSD), Nishath Verghese (ClearShape)
3:00-3:20pm	Break
3:20-5:00pm	Session 4: Waveform Modeling and Timing Analysis
	Advanced Modeling Techniques for Accurate Transistor-Level Timing Analysis Dmitry Messerman, Alex Gershtein, Sergey Goldenberg and Vladi Tsipenyuk
	Parameterized Waveform-Independent Gate Models for Timing and Noise Analysis Zhuo Feng and Peng Li

AccurateWaveform Modeling using Singular Value Decomposition with Applications to Timing Analysis Anand Ramalingam, Ashish Kumar Singh, Sani R. Nassif, Michael Orshansky and David Z. Pan
Fast and Accurate Waveform Analysis with Current Source Models Vineeth Thazhathu Veetil and Dennis Sylvester

Day 2 (February 27, 2007)

Time	Event
8:00 – 8:30	Registration / Breakfast
8:30 – 9:20	Session 5: SSTA-II Non-Linear Statistical Static Timing Analysis for Non-Gaussian Variation Sources Lerong Cheng, Jinjun Xiong and Lei He. Efficient variational interconnect modeling for statistical timing analysis by combined sensitivity analysis and model-order reduction Soroush Abbaspour, Revanta Banerji, Peter Feldmann and David Ling
9:20 – 10:10	Session 6: Variation-Tolerant Design Techniques Elastic Timing Scheme for Power-Efficient and Robust Performance Rupak Samanta, Ganesh Venkataraman, Nimay Shah and Jiang Hu On-line Failure Prediction and Its Application to Transistor Aging Mridul Agarwal, Bipul C. Paul and Subhasish Mitra
10:10 - 10:30	Break
10:30 -12:10	Special Session 7: What CAD Community Should Know about Emergent Reliability Challenges
	Joe McPherson (Texas Instruments) and Bruce McGaughy (Cadence)
12:10pm- 1:30pm	Lunch
1:30-2:35 pm	Session 8: Statistical Modeling of Process Data
	How to Construct Spatial Correlation Models: A Mathematical Approach Frank Liu
	Variogram based robust extraction of process variation Kaviraj Chopra, Narendra Shenoy and David Blaauw
	Mining test data for ranking cells in terms of timing uncertainties Pouria Bastani, Benjamin Lee, Li-C. Wang and Magdy Abadir
2:35-2:50pm	Break

2:50-4:05pm	Session 9: STA Methodology and Algorithms
	Enumerating the top-k aggressors set in delay-noise analysis Ravikishore Gandikota, Kaviraj Chopra, David Blaauw, Dennis Sylvester and Murat Becer.
	Static Timing: Back to Our Roots Ruiming Chen, Eric Foreman, Peter Habitz, Jeff Hemmett, Kerim Kalafala, Jeff Piaget, Peihua Qi, Natesan Venkateswaran, Chandu Visweswariah, Jinjun Xiong and Vladimir Zolotov
	A Fast Tolerance-based Incremental Timing Analysis Algorithm Kip Killpack