

2008 ACM/IEEE International Workshop on Timing Issues in the Specification and Synthesis of Digital Systems

The Portola Hotel at Monterey Bay, Monterey, California
February 25-26, 2008

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Sponsored by ACM/SIGDA and IEEE Circuits and Systems Society
Additional support from Cadence, IBM, Intel, Magma DA and Synopsys

ADVANCE PROGRAM

MONDAY, FEBRUARY 25, 2008

8:00 – 8:25am Registration and Breakfast

8:25 – 8:30am Welcome

N. Menezes (Intel)

8:30 – 10:10am Session I: Variational Timing Analysis

Chair: F. Dartu (Synopsys)

1. “A Framework for Block-Based Timing Sensitivity Analysis”

S. Kumar, C. Kashyap and S. Sapatnekar (Univ. of Minnesota and Intel)

2. “Efficient Monte Carlo based incremental statistical timing analysis”

V. Veetil, D. Sylvester and D. Blaauw (Univ. of Michigan)

3. “Parameterized Timing Analysis with General Delay Models and Arbitrary Variation Sources”

K. Heloue and F. Najm (Univ. of Toronto)

4. “Variational Waveform Propagation for Accurate Statistical Timing Analysis”

M. Schmidt, H. Kinzelbach and U. Schlichtmann (TU Muenchen and Infineon)

10:10 – 10:30am Break

10:30 – 12:10pm Session II: Noise Analysis

Chair: I. Keller (Cadence)

1. “Solving Logic Exclusivity (LE) Problem in Noise Analysis Using Gain Guided Backtracking Method”

R. Li, A.-J. Shey and M. Laudes (Sun Microsystems)

2. “False Noise Analysis Using Branch & Bound and SAT”

M. Palla, J. Bargfrede, K. Koch, W. Anbeier and R. Drechsler (Infineon and Univ. of Bremen)

3. “Constrained Aggressor Set Selection for Maximum Coupling Noise”

D. Sinha, S. Abbaspour and G. Schaeffer (IBM)

4. “Forbidden Transition Free Crosstalk Avoidance CODEC Design”

C. Duan, C. Zhu and S. Khatri (Texas A&M Univ.)

12:10 – 1:30pm Lunch

1:30 – 3:10pm Special Session: Multicore Computing

Invited talk: “Parallel computing technology: Can we PLEASE do it right this time?”

Tim Mattson, Application Research Lab, Intel

Invited talk: “The only future of CAD is parallel?”

Kurt Keutzer, UC-Berkeley

3:10 – 3:30pm Break

3:30 – 5:10pm Session III: Design Techniques

Chair: C. Chen (National Taiwan Univ.)

1. “Delay-Optimal Simultaneous Technology Mapping and Placement with Applications to Timing Optimization”

Y. Liu, R. Shelar and J. Hu (Texas A&M Univ. and Intel)

2. “Clock Distribution Scheme using Coplanar Transmission Lines”

V. Cordero and S. Khatri (Texas A&M Univ.)

3. “Figures of Merit to Characterize the Importance of Skin and Proximity Effects”

A. Shebaita, D. Petranovic and Y. Ismail (Northwestern Univ. and Mentor Graphics)

4. “Low-Power and High-Speed Interconnect Using Serial Passive Compensation”

C.-C. Liu and C.-K. Cheng (UCSD)

TUESDAY, FEBRUARY 26, 2008

7:30 – 8:00am Registration and Breakfast

8:00 – 9:15am Session IV: SSTA – Theory and Practice

Chair: P. Li (Texas A&M Univ.)

1. “Driver Waveform Computation for Timing Analysis with Multiple Voltage Threshold Driver Models”
P. Feldmann, S. Abbaspour, D. Sinba, G. Schaeffer, R. Banerji and H. Gupta (IBM)
2. “Singular Value Decomposition based Spatial Correlation Extraction for VLSI DFM Applications”
J.-H. Liu, L. Chen and C. Chen (National Taiwan Univ.)
3. “Modeling Crosstalk in Statistical Static Timing Analysis”
R. Gandikota, D. Blaauw and D. Sylvester (Univ. of Michigan)

9:20 – 10:35am Session V: Timing and Silicon Debug

Chair: Chirayu Amin (Intel)

1. “Diagnosis of Delay Defects and Delay Variations”
V. Mehta, M. Marek-Sadowska, K.-H. Tsai and J. Rajski (UCSB and Mentor Graphics)
2. “Speedpath Prediction Based on Learning from a Small Set of Examples”
P. Bastani, K. Killpack, L.-C. Wang and E. Chiprout (UCSB and Intel)
3. “Ranking of Unmodeled Systematic Timing Effects”
P. Bastani, N. Callegari, L.-C. Wang and M. Abadir (UCSB and Freescale)

10:35 – 10:50am Break

10:50 – 12:10pm Special Session: Parallel CAD Solutions

Invited talk: “Efficient Use of Multicore Processors for Timing Analysis,”

Joao Gueda, Chief Architect, CLK Design Automation

“A Multi-Algorithm Approach to Parallel Circuit Simulation”

X. Ye, D. Wei and P. Li (Texas A&M Univ.)

12:10 – 1:30pm Lunch

1:30 – 2:30pm Special Session: What Digital Designers Need to Know about Analog

Invited talk: “Microprocessor I/O Scaling Challenges,”

Bryan Casper, Intel

2:30 – 2:45pm Break

2:45 – 4:00pm Session VI: Reliability Challenges

Chair: C. Chen (National Taiwan Univ.)

1. “Optimized Circuit Failure Prediction for Aging: Practicality and Promise”
M. Agarwal, V. Balakrishnan, A. Bhuyan, K. Kim, M. Mizuno, B. C. Paul, W. Wang, Y. Cao and S. Mitra (Stanford and Arizona State Univ.)
2. “Delay Shifts Predict Gate-Oxide Early Life Failures”
T.-W. Chen, K. Kim, Y. Kim and S. Mitra (Stanford)
3. “A Fast, Analytical Estimator for the SEU-induced Pulse Width in Combinational Designs”
R. Garg, C. Nagpal and S. Khatri (Texas A&M Univ.)

TAU 2008 ORGANIZATION

General Chair: Noel Menezes (Intel)

TPC Chair: Frank Liu (IBM)

TPC members: Chirayu Amin (Intel)

Charlie C.-P. Chen (National Taiwan Univ.)

Floren Dartu (Synopsys)

Andrew Kahng (UCSD)

Igor Keller (Cadence Design Systems)

Peng Li (Texas A&M University)

Robert Mains (Sun Microsystems)

Farid Najm (University of Toronto)

Rajendran Panda (Freescale)

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