CALL FOR PAPERS – TAU 2019
ACM International Workshop on Timing Issues in the
Specification and Synthesis of Digital Systems

It has become clear that timing analysis is NO longer a solved problem, So, what are new challenges as
the industry embraces 10/7/5nm and below, rides the wave of ultra-low-power mobile, wearable
devices and jumps on the IoT handwagon? Are there new issues with older nodes, 16/28nm and up, in new
design use cases? How do we model timing/power interactions? How reliability requirements
coming from ADAS/IoT and related impact timing? How to apply AI/ML/BigData concepts and
techniques to the timing domain? How to meet the insatiable demands for accuracy, performance and
functionality? What are new fundamental challenges coming from process physics, 3D, variability,
voltage scaling, analog effects, mixed signal modeling and validation?

The TAU series of workshops provide an informal forum for practitioners and researchers working on
these and other temporal aspects of analog and digital systems to disseminate early work and engage in
a free discussion of ideas. The twenty-sixth in the TAU series, the TAU 2019 workshop invites
submissions and proposals from the traditional as well as emerging areas related to the timing
properties of digital electronic systems, including but not limited to the topics listed below.

Timing (including incremental timing)
- System-level timing
- Circuit/gate-level timing
- Transistor-level timing
- Timing of mixed signal circuits
- New types of latches, dual-edge devices, etc.

Modeling and simulation
- Transistor level modeling
- Analog circuit modeling
- Circuit level simulation
- Delay models and metrics
- Reliability modeling and simulation

Variability
- Timing analysis under variation and uncertainty
- Ultra-low voltage induced variation effects
- Statistical timing analysis and optimization
- Sensitivity/criticality analysis
- Yield analysis and optimization

Power, trade-offs and optimization
- Timing issues in low-power design
- Power-delay tradeoffs
- Identifying timing criticality in presence of voltage drop/supply/noise/variability
- Optimizing design in presence of non-constant supply (drop/noise/variability)

Characterization
- Efficient cell (library) characterization
- Variation effects and corner reductions
- Latch characterization
- Simulation and characterization of SRAM circuits

Clocking
- Complex clock trees and networks
- Clocking, synchronization, and skew
- Clock domains, static/dynamic logic
- Novel clocking schemes

Emerging technologies
- Full custom design analysis
- Special circuit families
- Timing issues for 3D ICs and TSVs
- New modeling techniques and machine learning
- Timing implications of emerging technologies

Others
- Integrated functional-temporal analysis
- Formal theories and methods
- Asynchronous systems
- Smart sensor placement
- FPGA Design and Analysis

Timing contest: As in prior years, TAU is organizing a timing contest. The topic for the TAU 2019 contest is
“Timing Driven Design Optimization”. Details are posted on the workshop website. Winners of the contest will be
awarded plaques as well as cash prizes!

SUBMISSION OF PAPERS

All papers must be submitted electronically via the workshop website www.tauworkshop.com. Submissions are
limited to 6 pages in the double column proceedings format. In order to allow for a blind review, submitted pdf
version of the papers should not contain the authors name or any direct reference to the authors. TAU is a
workshop aimed at fostering a high level of professional interaction, not a conference. Copies of papers will be
provided to the attendees, but the proceedings will not be published by the ACM or the IEEE. Therefore, accepted
papers can still be submitted to other conferences and journals.