Beyond CMOS
Superconductors, Spintronics, and More than Moore Enablers

Jamil Kawa, Synopsys Fellow
March 21, 2019
AGENDA

• Emerging Technology Trends
• Moore’s Law (for CMOS) is Struggling
• Alternative Technologies
  • Cold CMOS
  • Superconducting Electronics
  • Spintronics
• Quantum Computing
• Complementary Technologies
  • Photonics
• Summary & Conclusions
Emerging Technologies

“Trending” Buzzwords

• Quantum Supremacy
• Neuromorphic Computing
• Artificial Intelligence
• Autonomous Driving

Emerging Technologies

• In-memory Computing
• Cold CMOS
• Superconducting Electronics
• Spintronics
• PCMs
• ReRAMs / RRAMs
• Optical Communications
• Qubits
AGENDA

• Emerging Technology Trends
• **Moore's Law (for CMOS) is Struggling**
  • Alternative Technologies
    • Cold CMOS
    • Superconducting Electronics
    • Spintronics
  • Quantum Computing
  • Complementary Technologies
    • Photonics
• Summary & Conclusions
Scaling and Innovation

Innovation in materials and architecture pushed by reaching the limit of existing solutions

Cu
Strain
High-K
FinFET
Nanosheets
Si NanoWire

130nm
90nm
45nm
22nm
< 5nm
< 4nm
Technology Drivers

- **AI, Deep Machine Learning**
  - Computer driven sophisticated routines with high need for data crunching

- **Automotive**
  - A plethora of sensors making sensitive real-time driving decisions based on collected data
  - Complex communications system integrating a heterogeneous set of sensors, microprocessors, and communication devices

- **IoT**
  - IoT hyperconnectivity theme: hyperconnectivity value chain: sensing, communication, computing and storage, energy harvesting, security, services

- **Virtual Reality / Augmented Reality**
  - Virtual display of real and simulated environments ranging from gaming all the way through sophisticated military applications

**IBM's TrueNorth:** a 70mW reconfigurable processor with 1 million neurons, 256 million synapses, and 4096 parallel and distributed neural cores; designed for homogeneous scaling via native chip-to-chip communication.
Different Pathways Explored for 5nm and Beyond

- 7nm is Si finFET
- 5nm could be finFET or GAA nano-sheets
- III-V material is a big step
- TFET has promise. Has challenges too!
- NCFETs?
  - Lots of progress
- CNFETs?
  - Exciting and intriguing
  - Can it yield?
# Device Technology Milestones

<table>
<thead>
<tr>
<th>Tech Node (nm)</th>
<th>180</th>
<th>90</th>
<th>45</th>
<th>22</th>
<th>16/14</th>
<th>10</th>
<th>7</th>
<th>5</th>
<th>0.3</th>
</tr>
</thead>
<tbody>
<tr>
<td>Device</td>
<td>Planar SS 130 mV/V</td>
<td>Planar</td>
<td>Planar SS 130 mV/V</td>
<td>FinFET SS 80 mV/V</td>
<td>FinFET SS 70 mV/V</td>
<td>FinFET NCFET TFET</td>
<td>nano-sheets TFET V NW CNFET</td>
<td>Atom</td>
<td></td>
</tr>
<tr>
<td>Gate</td>
<td>Hi-K Gate last</td>
<td>Hi-K Gate last</td>
<td>Hi-K Gate last</td>
<td>Hi-K Gate last</td>
<td>Hi-K Gate last</td>
<td>GAA (gate all around)</td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Interconnect</td>
<td>Cu</td>
<td>Cu Low-k</td>
<td>Cu Low-k</td>
<td>Cu Low-k</td>
<td>Cu Low-k Air gap Low R contact</td>
<td>Cu Low-k Air gap Low R contact</td>
<td>Cu Low-k Air gap Low R contact</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Materials / Channel</td>
<td>LDD</td>
<td>LDD</td>
<td>Strain (SiN)</td>
<td>Ge Strain Complex Gate Stack</td>
<td>Ge Strain Complex Gate Stack</td>
<td>Creative Fin Doping</td>
<td>Creative Fin Doping III-V channel?</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
A Zoo of Scaling Boosters

**EVOLUTIONARY PROGRESS - DTCO SCALING**

**CELL LEVEL – SCALING BOOSTERS**

- MI/CPP gear ratio
- Partial Via landing
- Dual STI
- Single Diff. Break
- Self aligned Block
- Via jumper

- Open-MI architecture
- Super via
- Self-aligned gate contact
- M0A Pass-thru
- Fully self-aligned Vias
- FTUGC

Cell size impact  
Variability impact

Each booster is a one-node gain
CFETs: Stacking PMOS on Top of NMOS?

COMPLEMENTARY FET ARCHITECTURE (CFET)
MOVING THE N/P BOUNDARY IN THE VERTICAL DIRECTION

Cross section view

M0

Top electrode

Buried VDD

Buried VSS

Bottom electrode

Vss deep via

Vss shallow via

Buried Vdd

Buried Via
AGENDA

• Emerging Technology Trends
• Moore’s Law (for CMOS) is Struggling
• **Alternative Technologies**
  • Cold CMOS
  • Superconducting Electronics
  • Spintronics
• Quantum Computing
• Complementary Technologies
  • Photonics
• Summary & Conclusions
Cold CMOS – 77 Kelvin (-193 C)

Inspired by applications ranging from space exploration to CT scans
• Proven (including packaging and temp cycling) to 77K – liquid N temperature
• Have reliability concerns that can be managed
  – Including SOI
• Speed up can be used to operate at much lower VDD for same performance as 25C and very large energy savings

Pros
• Increased average carrier drift velocities (even at high fields)
• Steeper subthreshold slope, plus reduced subthreshold currents (channel leakages) which provide higher noise margins
• Higher transconductance
• Well-defined threshold voltage behavior
• No degradation of geometry effects
• Enhanced electrical line conductivity
• Dramatic increase in allowable current density limits

Si CMOS (bulk and SOI)
  – cooling improves: \(I_{\text{DS, sat}}, g_m, \mu_{\text{eff}}, S, I_{\text{off}}\)
  – cooling degrades: \(V_T\), hot carrier reliability
  – radiation tolerance: problem without RHBD
Cold CMOS cont’d

M. Elseworth: The Challenge of Operating Computers at Ultra-low Temperatures www.6sigmaet.info
Motivation of SCE's VLSI Target
CPU Clock Speed & Power Consumption

- CPU clock speed is leveling off at < 10 GHz
- Energy for world computing is projected to exceed production capacity by 2040
- Many innovations in CMOS like parallelism, low power, etc. have moved us forward….
- How much more runway?

Source: dynamize.com
The IARPA Challenge:
- To provide SCE EDA software supporting 1M gates/10M JJ
- To demonstrate a working processor, such as ARC, RISC 32/64, OpenSparc, or Leon3 (SparcV8) at 100GHz

CRITERIA:
- Support one or more SCE logic families, enable Scalability, QoR, Speed of Tool, flexibility to handle standards, multiple clocks

Taking SCE from “Hand Crafted” Circuits to the VLSI Era
The IARPA Challenge!
Superconductivity

• **Resistanceless** current flow
• **Quantization of flux** in a superconducting loop
  – Result of continuity of superconducting wavefunction*
  – Leads to flux ($\phi$)-phase ($\varphi$)* relation:

\[
\frac{\Delta \theta}{2\pi} = \frac{\Delta \phi}{\phi_0} = n, \quad \phi = \frac{\phi_0}{2\pi} \varphi
\]

• Single Flux Quantum (SFQ):
  \[
  \phi_0 = h/2e = 2.07 \times 10^{-15} \text{ Wb}
  \]

* Superconducting phase from quantum wavefunction
Josephson Junctions (JJ)

- Josephson Junction: two pieces of superconductor separated by a thin barrier:
  - Insulator, metal, ferromagnet, nanowire semiconductors, etc.
- Without any applied bias, a zero-resistance supercurrent \( I_S \) can flow across a JJ

\[
I_S = I_C \sin \phi
\]

\[
\Psi_1 = |\Psi_1| e^{i\phi_1}, \quad \Psi_2 = |\Psi_2| e^{i\phi_2}
\]

\[
\phi = (\phi_1 - \phi_2)
\]
Josephson Junction

• *Physically*: small break of superconducting wire

• **Two terminal, threshold device** (in SFQ circuits)
  – Critical current determined by geometry, material properties

• Two unique effects:
  – DC Josephson effect:  \( I = I_C \sin \varphi \)
  – AC Josephson effect:  \( V = \frac{\phi_0}{2\pi} \frac{\partial \varphi}{\partial t} = \frac{h}{2e} \frac{\partial \varphi}{\partial t} \)
Josephson Junction Basics

- JJs need biasing to keep them near switching threshold
- When a JJ is biased above $I_C$, the voltage across the junction is proportional to the time-derivative of the phase
- Magnetic flux quantum ejected from a superconducting loop through a Josephson junction can take the form of tiny voltage pulses. The presence or absence of a pulse in a given period of time can be used to perform computations.

**Single-Flux Quantum:**
Current in a superconducting loop containing a Josephson junction—a non-superconducting barrier generates a magnetic field with a tiny, quantized value.
RSFQ Circuit: JJ Operation

• When JJ threshold reached ($I > I_C$), creates voltage across junction

• Junctions are resistively-shunted
  – Quickly returns below $I_c$
    (to superconducting operation)

• Threshold behavior:
  Junctions emit voltage pulse.
  (Then returns to $I < I_C$)
Images of Superconducting QUBITS in the News

Photograph of superconducting circuit with nine qubits where, for the first time, the qubits are able to detect and effectively protect each other from bit errors (Photo credit: Julian Kelly). This Nature article has been featured in the New York Times, Wired, IEEE Spectrum, Nanotechweb, the Google Research Blog, and a UCSB press release.
Future of Memories – In Search of the Universal Memory

- DRAM and NAND, a $100B+ (2019) industry, will remain dominant.
- XPoint™, or ReRAM (if any), fits in as SCM and is likely to grow fast.
- STT-RAM is limited in density and will stay for niche applications.
- Racetrack memory will likely move from research to full production in the early 2020s.

Opportunities lie in filling the latency gaps + HDD replacement.
Giant Magnetoresistance (GMR)

\[ GMR = \frac{\Delta R}{R} = \frac{(R_{\uparrow\downarrow} - R_{\uparrow\uparrow})}{R_{\uparrow\uparrow}} \]

Albert Fert 1938-present

Peter Grunberg 1939-present

Nobel Prize in Physics 2007
Tunneling Magneto-resistance (TMR)

\[ TMR = \frac{G_P - G_{AP}}{G_{AP}} \]

- **TMR**: Tunneling magnetoresistance
- **FM**: Ferromagnetic
- **NM**: Nonmagnetic
- **\( G_P \)**: Parallel conductance
- **\( G_{AP} \)**: Antiparallel conductance

- The insulating tunnel barrier is a “spin filter”
- TMR > GMR allowing lower leakage and easier differential sensing making it better for memories
- Asymmetry: reversing the magnetic orientation of the free layer from anti-parallel to parallel is always harder
Four Spintronics Device Groups

GMR Valves  |  Magnetic Tunnel Junctions  |  Semiconductor Spintronic Devices  |  Spin Qubits

From Bora Nicolic course outline
Spintronics MRAM Progression

- **FIMS**: Field Induced Magnetic Switching 2002 ~ 2008
- **TAS**: Thermally Assisted Switching
- **STT**: Spin Transfer Torque
- **SOT**: Spin Orbit Torque
STT-RAM as Unified LP eNVM for IoT

- In a conventional memory sub-system, energy is consumed by several factors:
  - Fetch execution code from eFlash
  - Log back data to eFlash
  - Data access to a standalone flash
  - SRAM standby power, especially at very low duty cycles, typical of IoT operations
- STT-RAM can combine the working memory and NVM into a unified memory sub-system, drastically improving overall energy efficiency.

Source: Qualcomm & TDK, IEDM, 2015
Racetrack Memory

- Racetrack memory is a shift register type of memory
  - No direct bit access
- Writing: stray fields of the domains controlled by write current
- Reading: consecutive bits are shifted by the shifting current and are detected resistively by a GMR or a TMR scheme
- Resistive sensor detects stray fields of the domain walls
- Domain walls are “pinned” by notches in the tracks
  - The DW stays preferentially within the notches because it is a low state of energy
- Memory needs one transistor per ~ 100 bits
Summing Up Spintronics in One Slide

- **Features**
  - NM metal
  - SOT (Spin Orbital Torque)
  - S1 and S2 layers
  - Electron flow and torque
  - Ferromagnetic layers
  - Spacer
  - Electromagnetic wave
  - Racetrack Storage Array
  - Shifting current
  - Resistive sensor

- **Equations**

  \[
  \frac{\partial m}{\partial t} = -y m \times H_{eff} + \alpha m \times \frac{\partial m}{\partial t} + \tau
  \]

- **Concepts**
  - Current induced SOT
  - Spin orbital torque (SOT)
  - Write current
AGENDA

• Emerging Technology Trends
• Moore’s Law (for CMOS) is Struggling
• Alternative Technologies
  • Cold CMOS
  • Superconducting Electronics
  • Spintronics
• Quantum Computing
• Complementary Technologies
  • Photonics
• Summary & Conclusions
Beyond Academic Curiousness, Does Anybody Care?

No small effort
Estimated annual spending on non-classified quantum-technology research, 2015, €m

Source: McKinsey

Source Economist, technology quarterly March 2017
Locking Intellectual Rights to QC Related Inventions

**Excited states**
Patent applications to 2015, in:

**Quantum computing**
- United States 295
- Canada 79
- Japan 78
- Britain 36
- China 29
- Australia 26
- Germany 22
- South Korea 11
- Israel 9
- Finland 7

**Quantum cryptography**
- China 367
- United States 233
- Japan 100
- Britain 50
- Malaysia 31
- South Korea 27
- Germany 24
- France 15
- Australia 14
- Canada 11
- Italy 11

**Quantum sensors**
- United States 105
- China 104
- Germany 25
- Japan 18
- Britain 12
- Canada 6
- Israel 6
- France 5
- Australia 3
- South Korea 2
- Russia 2
- Taiwan 2

**Quantum-key distribution**
Patent applications by country*

Sources: UK Intellectual Property Office; European Commission

*By location of corporate headquarters

Source: Economist, technology quarterly March 2017
<table>
<thead>
<tr>
<th>Technology</th>
<th>Manifestation</th>
<th>Coherence Time</th>
<th>Logic Success Rate</th>
<th>Number of Entangled Qubits</th>
<th>Companies</th>
<th>Universities &amp; National Labs</th>
<th>Notes</th>
</tr>
</thead>
<tbody>
<tr>
<td>Silicon Spin</td>
<td></td>
<td>.03-30s</td>
<td>99.00%</td>
<td>2.00</td>
<td>Intel, HRL</td>
<td>UNSW, U. of Wisconsin, TU Delft, Princeton, Sandia, National Labs, Riken</td>
<td>3 varieties @ UNSW alone!</td>
</tr>
<tr>
<td>Superconducting Loops</td>
<td></td>
<td>.00005 s</td>
<td>99.40%</td>
<td>9.00</td>
<td>Google, IBM, Intel, Quantum Circuits, Dwave, Rigetti</td>
<td>UC Santa Barbara, ETH Zurich, TU Delft, Yale, UC Berkeley, MIT/Lincoln Labs</td>
<td></td>
</tr>
<tr>
<td>Ion Traps</td>
<td></td>
<td>1000s</td>
<td>99.90%</td>
<td>14.00</td>
<td>ionQ</td>
<td>U of Innsbruck, US Nat'l Institute of Standards, Oxford, U. of Maryland, MIT, U of Sussex</td>
<td></td>
</tr>
<tr>
<td>Diamond Vacancies</td>
<td></td>
<td>2s</td>
<td>99.20%</td>
<td>2.00</td>
<td>Quantum Diamond Technology</td>
<td>TU Delft, U of Stuttgart, U of Chicago, Harvard, USTC Hefei</td>
<td>New</td>
</tr>
<tr>
<td>Topological Qubits</td>
<td></td>
<td>untested</td>
<td>none to date</td>
<td>none to date</td>
<td>Microsoft, Bell Labs</td>
<td>TU Delft, Niels Bohr Institute</td>
<td>New</td>
</tr>
</tbody>
</table>
QUBIT Current Realizations

- Silicon spin qubit
  - Nature communications
- Trapped Ion QUBIT
  - Sergey Frolov, U Pittsburg
- Superconductor Loop
  - Franco Nori
- Trapped Ion
  - APS / Alan Stonebraker
    - Jugsang Kim article, Duke University
- Diamond N Vacancy
  - Quantum Engineering Group, MIT
- Topological QUBITs
  - Quantum magazine
Where Do We Stand?
Google “Bristlecone”, 72 Qubits
“Quantum Supremacy Can Be Comfortably Demonstrated with 49 Qubits, a Circuit Depth Exceeding 40, and a Two-Qubit Error Rate Below 0.5%”
AGENDA

• Emerging Technology Trends
• Moore’s Law (for CMOS) is Struggling
• Alternative Technologies
  • Cold CMOS
  • Superconducting Electronics
  • Spintronics
• Quantum Computing
• Complementary Technologies
  • Photonics
• Summary & Conclusions
Silicon Photonics
A Class of Devices that Exploits Silicon as Optical Medium

- Photonics is the branch of physics that studies light generation, detection, and manipulation through emission, transmission, modulation, signal processing, switching, amplification, and detection/sensing; the goal of photonics is to use light to perform functions that traditionally fall within the electronics domain
  - Silicon Photonics is the study and application of photonic systems which use silicon as an optical medium

- Photonic Integrated Circuits (PIC) can be manufactured using either standard silicon process technologies, or using III-V processes in indium phosphide (InP)
  - Monolithic integration does require a re-design of CMOS process

- Hybrid devices can be implemented in which the photonic (PIC) and electronic (EIC) components are integrated onto a single die, or by means of 3D-IC solutions
  - The advances in 3D-IC integration could allow for the independent evolution of EIC and PIC, both w.r.t. the process technology and the design tools
Silicon Photonics

3D-IC Integrated Transmitter IC : EIC Flip-Chip’d Onto PIC Interposer
PIC Interposer Wire-Bonded to Package

Silicon Photonics Roadmap
*From Board-Level to Passive to Active Interposer*

Source: F. Benetti, STMicroelectronics Investor Day 2017
Photonics Snapshot

Deep Rib Ring Resonators; Source: F. Boeuf, STMicroelectronics, 2017
AGENDA

• Emerging Technology Trends
• Moore’s Law (for CMOS) is Struggling
• Alternative Technologies
  • Cold CMOS
  • Superconducting Electronics
  • Spintronics
• Quantum Computing
• Complementary Technologies
  • Photonics
• **Summary & Conclusions**
Summary & Conclusions

- Moore’s Law for CMOS is well and alive beyond 5nm but with diminishing returns
- Technology drivers are mainly AI, Big Data, Cloud Computing, BlockChain, Autonomous Driving and Augmented reality
  - Need for high bandwidth communications, high REAL TIME decision computational power at low energy budget
- Quantum computing is getting a big buzz but is still far from reality
  - Quantum supremacy
- Many alternative and complementary technologies are competing and/or complementing one another for solutions
  - Spintronics
  - Cold CMOS
  - Superconducting
  - Photonics